TPS2373 High-Power PoE PD Interface with Advanced Startup

1 Features

- IEEE 802.3bt (Draft) PD Solution for Type 3 or Type 4 PoE
- Supports Power Levels for Type-4 (TPS2373-4) 90-W and Type-3 (TPS2373-3) 60-W Operation
- Robust 100 V Hotswap MOSFET
  - TPS2373-4 (typ.): 0.1-Ω, 2.2-A Current Limit
  - TPS2373-3 (typ.): 0.3-Ω, 1.8-A Current Limit
- Allocated Power Indicator Outputs
- Advanced Startup for DC-DC
  - Simplifies Downstream DC-DC Design
  - Compliant to PSE Inrush
- Automatic Maintain Power Signature (MPS)
  - Auto-adjust MPS for Type 1-2 or 3-4 PSE
  - Supports Ultra-Low Power Standby Modes
- Primary Adapter Priority Input
- Supports PoE++ PSE
- -40°C to 125°C Junction Temperature Range
- 20-lead VQFN Package

2 Applications

- IEEE 802.3bt (Draft) Compliant Devices
- 4PPOE
- Pass-through System
- Security Cameras
- Multiband access points
- Pico-base Stations
- Video and VoIP Telephones
- Systems using Redundant Power Feeds

3 Description

The TPS2373 contains all of the features needed to implement an IEEE802.3at or IEEE802.3bt (draft) (Type 1-4) powered device (PD). The low internal switch resistance allows the TPS2373-4 and TPS2373-3 to support high power applications up to 90 W and 60 W respectively. Assuming 100-meter CAT5 cable, this translates into 71.3 W and 51 W at PD input.

The TPS2373 operates with enhanced features.

The Advanced Startup function for DC-DC results in a simple, flexible, and minimal system cost solution, while ensuring that IEEE802.3bt (draft) startup requirements are met. It helps to reduce the size of the low voltage bias capacitor considerably. It also allows long DC-DC converter soft-start period and enables the use of a low-voltage PWM controller.

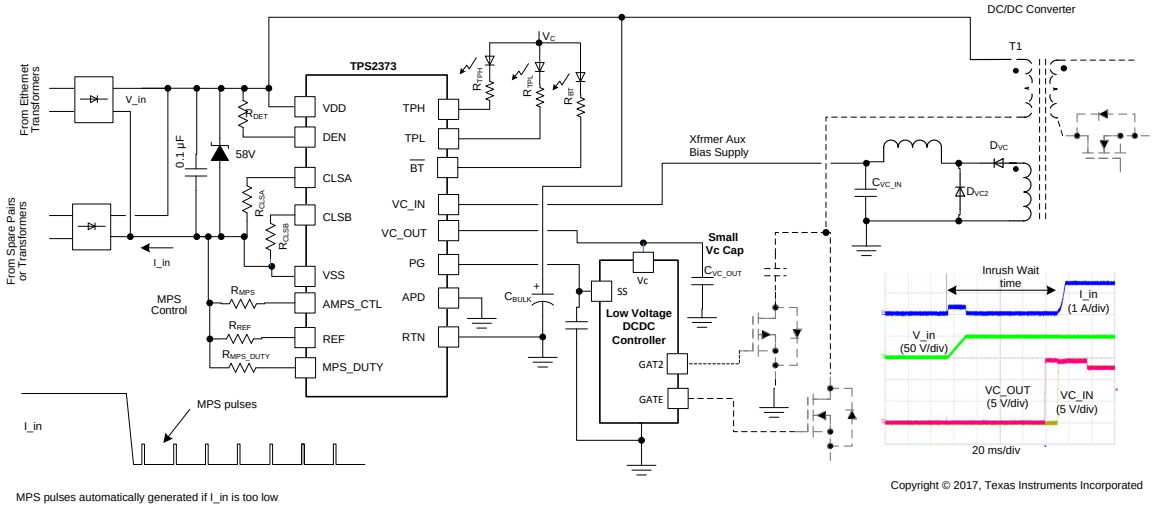
The Automatic MPS function enables applications requiring very low power standby modes. The TPS2373 automatically generates the necessary pulsed current to maintain the PSE power. An external resistor is used to enable this functionality and to program the MPS pulsed current amplitude.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2373	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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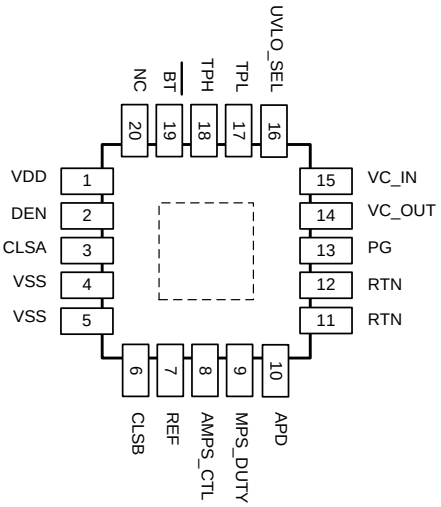
4 Revision History

DATE	REVISION	NOTES
April 2017	*	Advance Information release.
June 2017	*	Production Data release.

5 Pin Configuration and Functions

VQFN
20-Pin RGW Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Connect to positive PoE input power rail. Bypass with 0.1 µF to VSS.
DEN	2	I/O	Connect a 24.9 kΩ resistor from DEN to VDD to provide the PoE detection signature. Pull DEN to VSS to disable the pass MOSFET during powered operation.
CLSA	3	O	Connect a resistor from CLSA to VSS to program the first classification current.
VSS	4, 5	—	Connect to negative power rail derived from PoE source.
CLSB	6	O	Connect a resistor from CLSB to VSS to program the second classification current.
REF	7	O	Internal 1.5 V voltage reference. Connect a 49.9kΩ_1% resistor from REF to VSS.
AMPS_CTL	8	O	Automatic MPS control. Connect a resistor with appropriate power rating (to support the MPS current) from AMPS_CTL to VSS to program the MPS current amplitude. Leave AMPS_CTL open to disable the automatic MPS function.
MPS_DUTY	9	I	MPS duty cycle select input, referenced to VSS, internally driven by a precision current source with voltage limited to less than ~5.5V. A resistor connected to VSS determines if the MPS duty cycle selected is either 5.4% (open), 8.1% (~60.4 kΩ) or 12.5% (short).
APD	10	I	Auxiliary power detect input. Raise 1.65 V above RTN to disable pass MOSFET, to force TPH active (low) and to force TPL and /BT inactive (open). If not used, connect APD to RTN.
RTN	11, 12	—	Drain of PoE pass MOSFET. Return line from the load to the controller.
PG	13	O	Power Good output. Open-drain, active-high output referenced to RTN.
VC_OUT	14	O	VC output. Connect to the low voltage supply pin of the PWM controller. Bypass with a 1 µF to RTN in most applications. If the applications requires operations from a 12 V adapter, a higher capacitance value is needed.
VC_IN	15	I	VC input. Connect to auxiliary bias voltage source, usually derived from an auxiliary winding of the power transformer of the converter. Bypass with a 0.1 µF to RTN.
UVLO_SEL	16	I	UVLO select, referenced to RTN, internally pulled-up to 5.5 V internal rail. Leave open when the selected PWM has a falling UVLO above 7.25V. Pull UVLO_SEL low if it is between 4.25V and 7.25V.
TPL	17	O	PSE allocated power outputs, binary coded. Open-drain, active-low outputs referenced to RTN. TPL becomes open and TPH pulls low if an auxiliary power adapter is detected via the APD input.
TPH	18	O	
$\overline{BT}$	19	O	Indicates that a PSE applying an IEEE802.3bt (Type 3 or 4) mutual identification scheme has been identified. Open-drain, active-low output referenced to RTN. /BT becomes open if an auxiliary power adapter is detected.
NC	20	—	No connect pin. Leave open.
Pad	—	—	The exposed thermal pad must be connected to VSS. A large fill area is required to assist in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over recommended T_J range; voltages with respect to V_{VSS} (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VDD, DEN	–0.3	100	V
	RTN(2)	–0.6	100	
	VC_IN to RTN	–0.6	25	
	APD to RTN	–0.3	6.5	
	UVLO_SEL to RTN	–0.3	6.5	
Output voltage	CLSA, CLSB, REF, MPS_DUTY(3)	–0.3	6.5	V
	VC_OUT to RTN	–0.3	20	
			$V_{VDD-RTN}$+0.3	
	AMPS_CTL(3)	–0.3	30	
Voltage	PG to RTN	–0.3	100	V
	TPH, TPL, $\overline{BT}$ to RTN	–0.3	100	
Sinking current	RTN(4)	Internally limited		mA
	PG, TPH, TPL, $\overline{BT}$		10	
	DEN		1	
Sourcing current	VC_OUT startup	Internally limited		mA
	VC_OUT operational mode		60	
	CLSA, CLSB		65	
	REF	Internally limited		
	AMPS_CTL		50	
$T_{J(max)}$	Maximum junction temperature	Internally limited		°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With $I_{(RTN)}$ = 0
(3) Do not apply voltages to these pins
(4) SOA limited to RTN = 80 V at 2.5 A.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	
		IEC 61000-4-2 contact discharge(3)	±8000	
		IEC 61000-4-2 air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Discharges applied to circuit of Figure 30 between RJ-45, adapter, and output voltage rails, on TPS2373-4EVM-758.

6.3 Recommended Operating Conditions

over operating free-air temperature range and voltages with respect to V_{SS} (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	RTN, VDD	0		57	V
	APD to RTN	0		5	V
	VC_IN to RTN	0		15	
Voltage range	TPH, TPL, $\overline{BT}$ to RTN	0		57	V
	PG to RTN	0		57	
Sinking current	RTN (TPS2373-3)			1.2	A
	RTN (TPS2373-4)			1.85	
	PG, TPH, TPL, $\overline{BT}$			3	mA
Sourcing current	VC_OUT			20	mA
Resistance	CLSA, CLSB(1)	60			Ω
	AMPS_CTL(1)	1			kΩ
	REF(1)	48.9	49.9	50.9	
	APD to RTN			200	
Junction temperature		–40		125	°C

(1) Voltage should not be externally applied to this pin.

6.4 Thermal Information

THERMAL METRIC(1)		TPS2373-3 RGW (VQFN) 20 PINS	TPS2373-4 RGW (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.2	38.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.6	28.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	16.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.8	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, 40 V ≤ V_{VDD} ≤ 57 V; R_{DEN} = 24.9 kΩ; PG, CLSA, CLSB, MPS_DUTY, AMPS_CTL, UVLO_SEL, VC_IN, TPH, TPL and $\overline{BT}$ open; APD connected to RTN; C_{VC_OUT} = 1 µF; R_{REF} = 49.9 kΩ; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DETECTION (DEN)							
	Bias current	DEN open, V_{VDD} = 10.1 V, Measure I_{SUPPLY}(VDD, RTN, DEN), Not in mark		3	4.8	14	µA
	DEN leakage current	V_{DEN} = V_{VDD} = 57 V			0.5	5	µA
	Detection current	Measure I_{SUPPLY}(VDD, RTN, DEN), V_{VDD} = 1.4 V		53.8	56.5	58.3	µA
		Measure I_{SUPPLY}(VDD, RTN, DEN), V_{VDD} = 10.1 V, Not in mark		395	410	417	
V_{PD_DIS}	Disable threshold	DEN falling		3	3.7	5	V
	Hysteresis			75	150	250	mV
AUXILIARY POWER DETECTION (APD)							
V_{APDEN}	Voltage threshold	V_{APD} rising, measure to V_{RTN}		1.45	1.65	1.82	V
V_{APDH}		Hysteresis, measure to V_{RTN}			0.09		
	Pulldown resistance	$V_{(APD–RTN)}$ = 5 V, measure R_{APD}			2.8		MΩ
CLASSIFICATION (CLS)							
I_{CLS}	Classification A,B signature current	13 V ≤ V_{VDD} ≤ 21 V, Measure I_{VDD} + I_{DEN} + I_{RTN}					
		R_{CLSA} or R_{CLSB} = 1210 Ω		2.1	2.5	2.9	mA
		R_{CLSA} or R_{CLSB} = 249 Ω		9.9	10.6	11.2	
		R_{CLSA} or R_{CLSB} = 140 Ω		17.6	18.6	19.4	
		R_{CLSA} or R_{CLSB} = 90.9 Ω		26.5	27.9	29.3	
		R_{CLSA} or R_{CLSB} = 63.4 Ω		38	39.9	42	
V_{CL_ON}	Class lower threshold	V_{VDD} rising, I_{CLS} ↑		11.9	12.5	13	V
V_{CL_H}		Hysteresis		1.4	1.6	1.7	
V_{CU_ON}	Class upper threshold	V_{VDD} rising, I_{CLS}↓		21	22	23	V
V_{CU_H}		Hysteresis		0.5	0.78	0.9	
V_{MSR}	Mark reset threshold	V_{VDD} falling		3	3.9	5	V
	Mark state resistance	2-point measurement at 5 V and 10.1 V		6	10	12	kΩ
	Leakage current	V_{VDD} = 57 V, V_{CLS} = 0 V, measure I_{CLS}				1	µA
t_{LCF_PD}	Long first class event timing	Class 1st event time duration for new MPS		76	81.5	86	ms
PASS DEVICE (RTN)							
$r_{DS(on)}$	On resistance		TPS2373-3		0.3	0.55	Ω
			TPS2373-4		0.1	0.2	
	Input bias current	V_{VDD} = V_{RTN} = 30 V, measure I_{RTN}				50	µA
	RTN leakage current	V_{VDD} = V_{RTN} = 100 V, V_{DEN} = V_{VSS} , measure I_{RTN}				80	
	Current limit	V_{RTN} = 1.5 V	TPS2373-3	1.55	1.8	2.05	A
		V_{RTN} = 1.5 V	TPS2373-4	1.9	2.2	2.5	
	Inrush current limit	V_{RTN} = 2 V, V_{VDD}: 20 V → 48 V	TPS2373-3	165	200	237	mA
		V_{RTN} = 2 V, V_{VDD}: 20 V → 48 V	TPS2373-4	275	335	395	
	Inrush termination	Percentage of inrush current		80%	90%	99%	
t_{INR_DEL}		Inrush delay		78	81.5	87	ms
	Foldback threshold	V_{RTN} rising		12.5	14.5	15.5	V
	Foldback deglitch time	V_{RTN} rising to when current limit changes to inrush current limit		1.35	1.65	1.95	ms

Electrical Characteristics (continued)

Unless otherwise noted, 40 V ≤ V_{VDD} ≤ 57 V; R_{DEN} = 24.9 kΩ; PG, CLSA, CLSB, MPS_DUTY, AMPS_CTL, UVLO_SEL, VC_IN, TPH, TPL and $\overline{BT}$ open; APD connected to RTN; C_{VC_OUT} = 1 µF; R_{REF} = 49.9 kΩ; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PG)						
	Output low voltage	Measure V_{PG} – V_{RTN}, I_{PG} = 2 mA, V_{RTN} = 2 V, V_{DD}: 20 V → 48 V		0.27	0.5	V
	Leakage current	V_{PG} = 57 V, V_{RTN} = 0 V			10	µA
		V_{PG} = 10 V, V_{RTN} = 0 V			1	
PSE TYPE INDICATION (TPL, TPH, $\overline{BT}$)						
V_{TPL}	Output low voltage	I_{TPL} = 2 mA, after 2-, 3- or 5-event classification, startup has completed, V_{RTN} = 0 V		0.27	0.5	V
V_{TPH}	Output low voltage	I_{TPH} = 2 mA, after 4- or 5-event classification, startup has completed, V_{RTN} = 0 V		0.27	0.5	
V_{BT}	Output low voltage	I_{BT} = 2 mA, after IEEE802.3bt classification, startup has completed, V_{RTN} = 0 V		0.27	0.5	
	Leakage current	V_{TPL} or V_{TPH} or V_{BT} = 7 V, V_{RTN} = 0 V			1	µA
t_{TPLHBT}	TPL, TPH, $\overline{BT}$ delay	From VC_IN high with PG open during startup to TPH and/or TPL and/or $\overline{BT}$ active	20	24	28	ms
UVLO						
V_{UVLO_R}	UVLO rising threshold	V_{VDD} rising	36.3	38.1	40	V
V_{UVLO_F}	UVLO falling threshold	V_{VDD} falling	30.5	32	33.6	
V_{UVLO_H}	UVLO hysteresis			6.1		V
BIAS CURRENT						
	Operating current	40 V ≤ V_{VDD} ≤ 57 V, startup has completed		550	800	µA
STARTUP						
V_{VCO_UV}	VC_OUT undervoltage falling threshold	$V_{VC\_OUT-RTN}$ falling	6.45	6.9	7.35	V
		$V_{VC\_OUT-RTN}$ falling, UVLO_SEL connected to RTN	3.45	3.9	4.25	
$V_{VCO\_UV\_H}$	VC_OUT undervoltage hysteresis			0.42		
		UVLO_SEL connected to RTN		0.046		
I_{VCOUT}	Startup current source	$V_{APD-RTN}$ = 2.5 V				mA
		V_{VDD} ≥ 28 V, $V_{VC\_OUT-RTN}$ = 13.6 V	21.5	26	29	
		V_{VDD} ≥ 10 V, $V_{VC\_OUT-RTN}$ = 7 V	8	12.5	19	
		V_{VDD} ≥ 8 V, $V_{VC\_OUT-RTN}$ = 6.5 V	3.9	6.3	9.7	
V_{VC_ST}	VC_OUT startup voltage	Measure V_{VC_OUT} during startup, I_{VC_OUT} = 0 mA	13.8		15	V
		Measure V_{VC_OUT} during startup, I_{VC_OUT} = 22 mA	13.5		15	V
V_{UVLO_SE}	VC_OUT UVLO select threshold	to RTN	1.8	2.1	2.3	V
	UVLO_SEL pullup current		14	20	25	µA
V_{VCIN_ON}	VC_IN rising threshold to turn on the VC switch	to RTN	8	8.5	9	V
r_{VC}	VC switch on resistance	$V_{APD-RTN}$ = 2.5 V				Ω
		V_{VDD} ≥ 28 V, V_{VC_IN-RTN} = 10 V			13.3	
		V_{VDD} ≥ 20 V, V_{VC_IN-RTN} = 10 V			15.5	
t_{STUP_OFF}	Startup current source turn off delay and TPH, TPL, $\overline{BT}$ turn on delay	From when the VC switch turns on	20	24	28	ms
t_{STUP_OUT}	Startup current source time out	From startup source turn on to turn off	47.5	50	53	ms

Electrical Characteristics (continued)

Unless otherwise noted, 40 V ≤ V_{VDD} ≤ 57 V; R_{DEN} = 24.9 kΩ; PG, CLSA, CLSB, MPS_DUTY, AMPS_CTL, UVLO_SEL, VC_IN, TPH, TPL and $\overline{BT}$ open; APD connected to RTN; C_{VC_OUT} = 1 µF; R_{REF} = 49.9 kΩ; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MPS						
	MPS DC supply current	Startup has completed, I_{RTN} = 0 mA			0.8	mA
	AMPS_CTL pulsed voltage	Startup has completed, I_{RTN} < 20 mA, R_{MPS} = 1 KΩ to 12 kΩ	23.1	24	24.9	V
	Automatic MPS falling current threshold	Startup has completed, I_{RTN} threshold to generate AMPS_CTL pulses	21.5	28	34.5	mA
		Hysteresis on RTN current		1		
	MPS pulsed mode duty cycle for Type 1-2 PSE	MPS pulsed current duty cycle	25.8%	26.1%	26.4%	
		MPS pulsed current ON time	76	81.5	87	ms
		MPS pulsed current OFF time		230	250	
	MPS pulsed mode duty cycle for Type 3-4 PSE	MPS pulsed current duty cycle, R_{MPS_DUTY} > 230 kΩ	5.2%	5.43%	5.6%	
		MPS pulsed current ON time, R_{MPS_DUTY} > 230 kΩ	14.5	15.0	15.7	ms
		MPS pulsed current duty cycle, R_{MPS_DUTY} < 8 kΩ	12.3%	12.5%	12.7%	
		MPS pulsed current ON time, R_{MPS_DUTY} < 8 kΩ	36	37.5	39	ms
		MPS pulsed current duty cycle, 43 kΩ < R_{MPS_DUTY} < 77 kΩ	7.9%	8.1%	8.3%	
		MPS pulsed current ON time, 43 kΩ < R_{MPS_DUTY} < 77 kΩ	22.2	23.1	24	ms
		MPS pulsed current OFF time, R_{MPS_DUTY} from 0 Ω to open circuit	250	263.5	277	ms
	MPS_DUTY pullup current		14	17	20	µA
THERMAL SHUTDOWN						
	Shutdown	T_J↑	140	150		°C
	Hysteresis (1)			20		°C

(1) Parameters provided for reference only, and do not constitute part of TI published specifications for purposes of TI product warranty.

6.6 Typical Characteristics

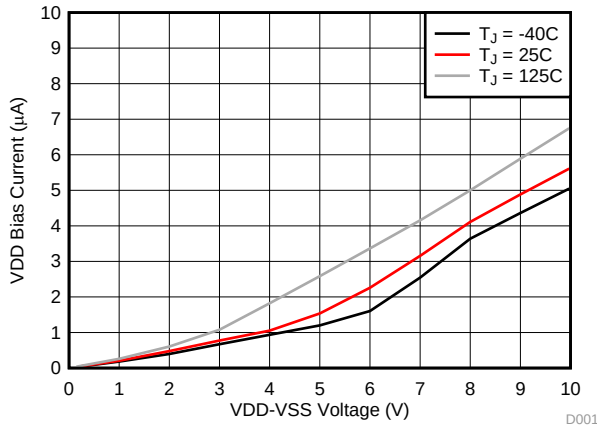


Figure 1. Detection Bias Current vs PoE Voltage

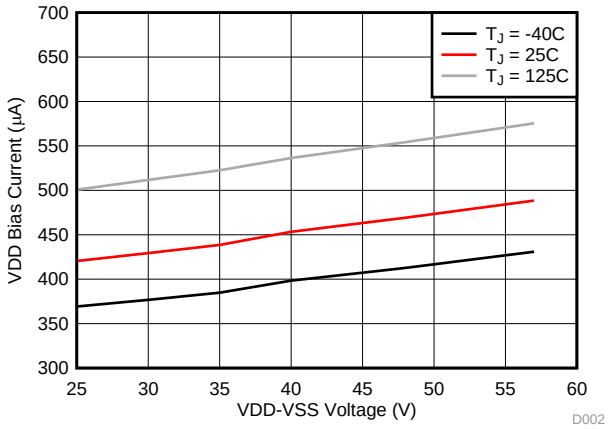


Figure 2. I_{VDD} Bias Current vs Voltage

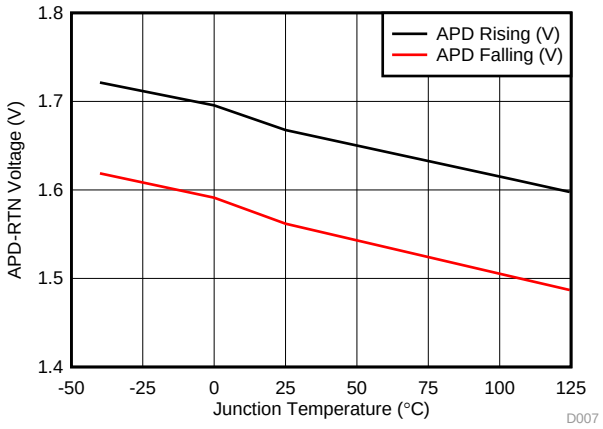


Figure 3. APD Threshold Voltage vs Temperature

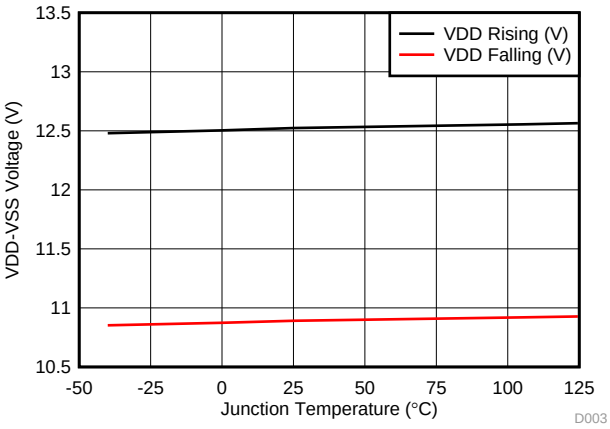


Figure 4. Classification Lower Threshold vs Temperature

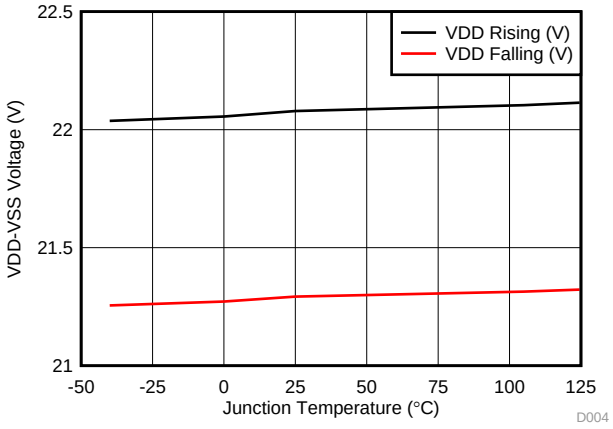


Figure 5. Classification Upper Threshold vs Temperature

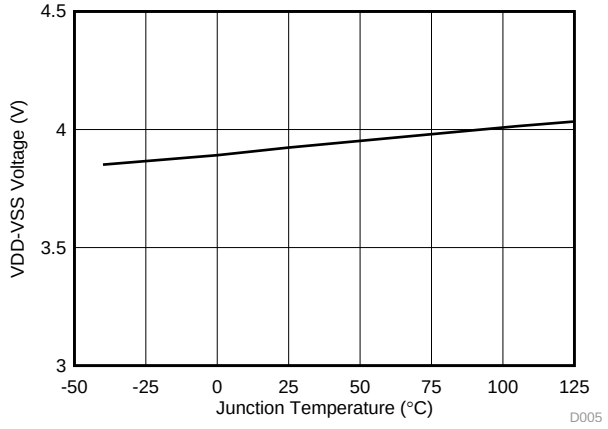


Figure 6. Mark Reset Threshold vs Temperature

Typical Characteristics (continued)

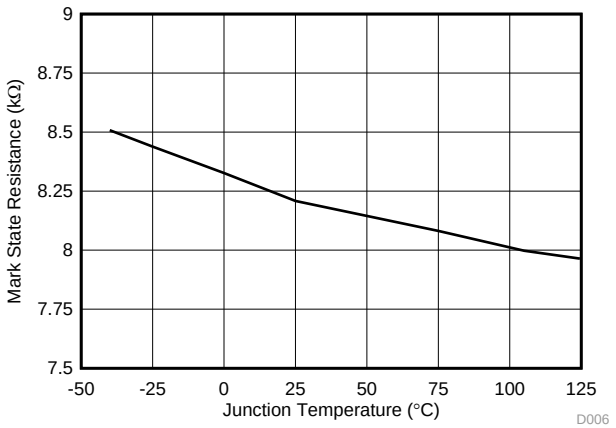


Figure 7. Mark Resistance vs Temperature

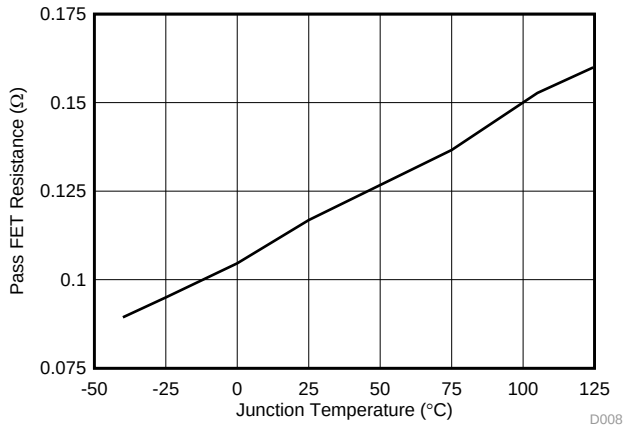


Figure 8. Pass FET Resistance vs Temperature, TPS2373-4

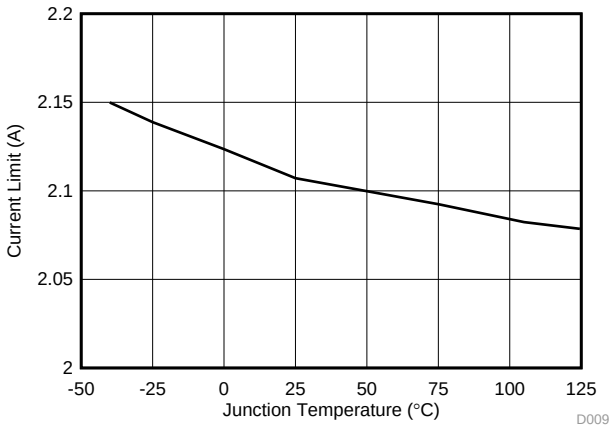


Figure 9. PoE Current Limit vs Temperature, TPS2373-4

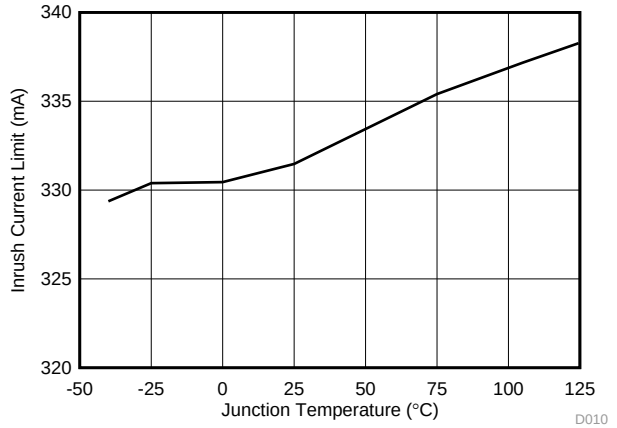


Figure 10. PoE Inrush Current Limit vs Temperature, TPS2373-4

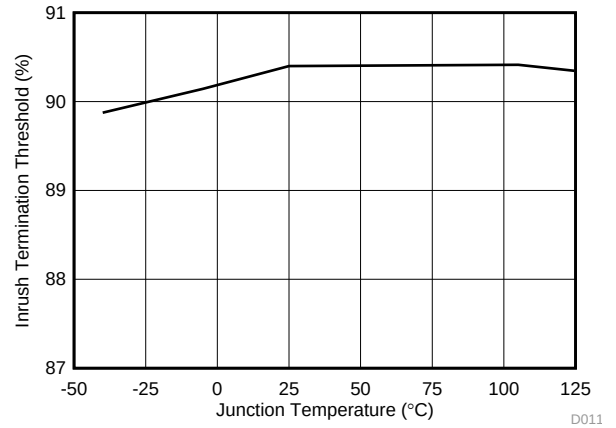


Figure 11. Inrush Termination Threshold vs Temperature

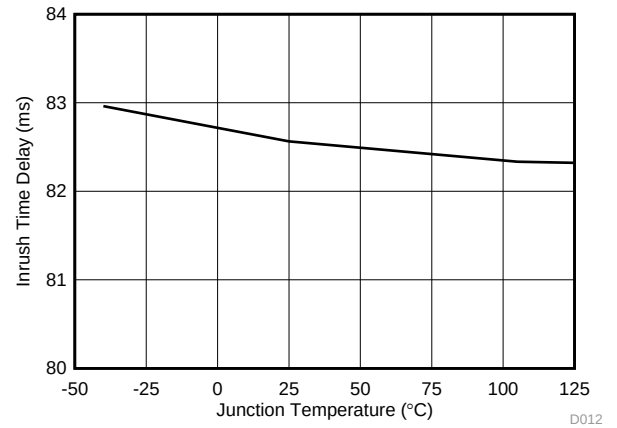


Figure 12. Inrush Time Delay vs Temperature

Typical Characteristics (continued)

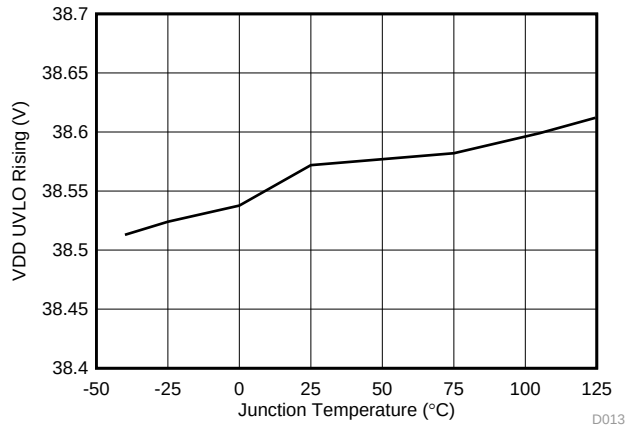


Figure 13. UVLO Rising Threshold vs Temperature

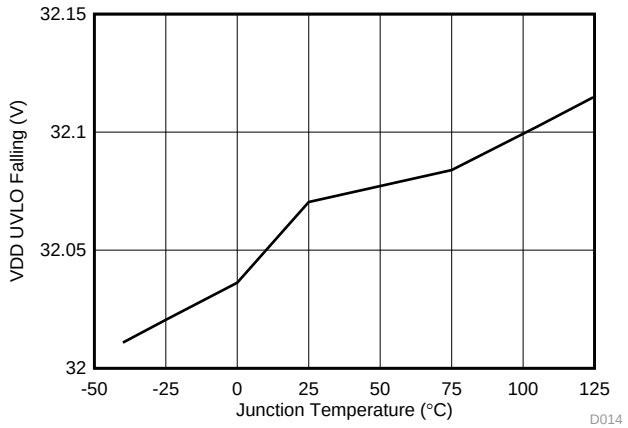


Figure 14. UVLO Falling Threshold vs Temperature

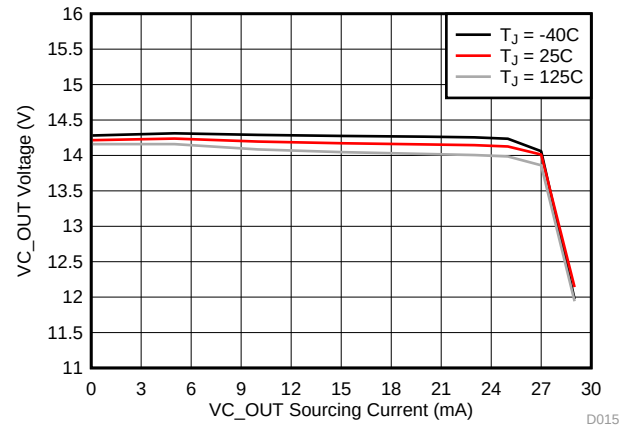


Figure 15. Converter Startup Voltage vs Current

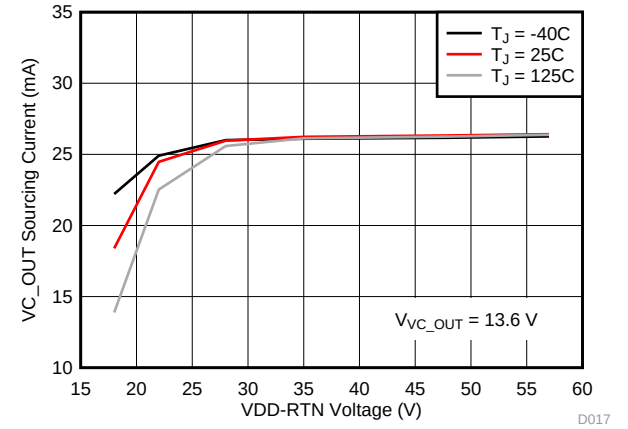


Figure 16. Converter Startup Current vs Input Voltage

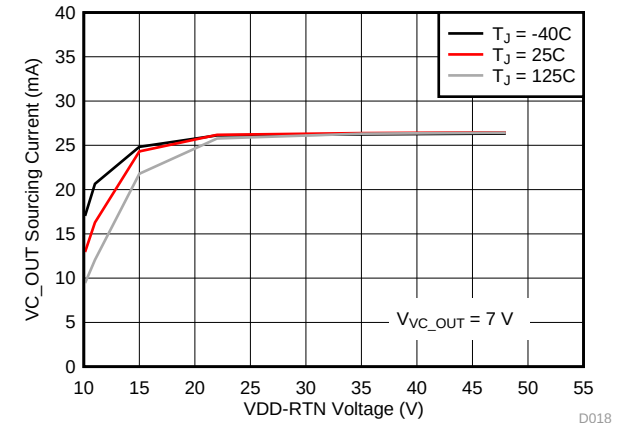


Figure 17. Converter Startup Current vs Input Voltage

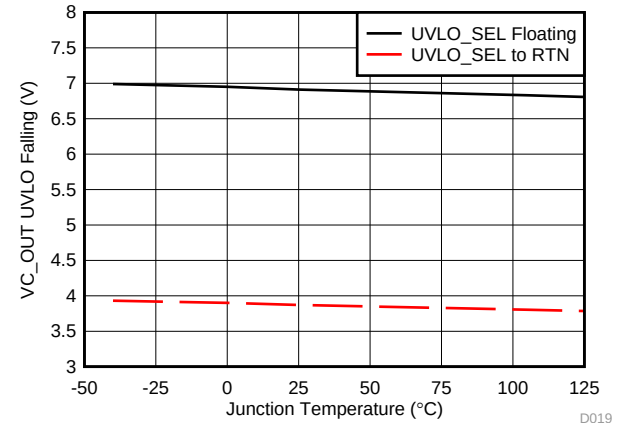


Figure 18. VC_OUT UVLO vs Temperature

Typical Characteristics (continued)

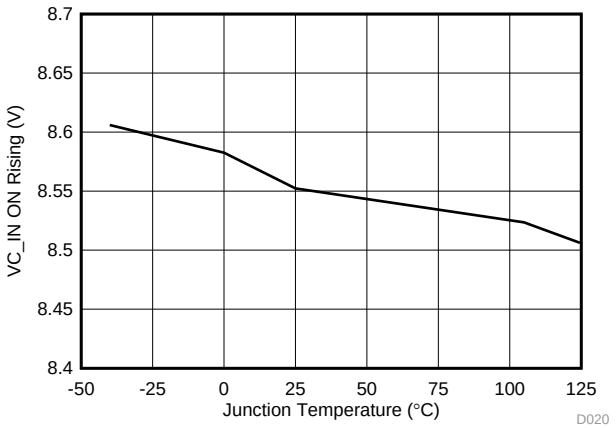


Figure 19. VC_IN Threshold vs Temperature

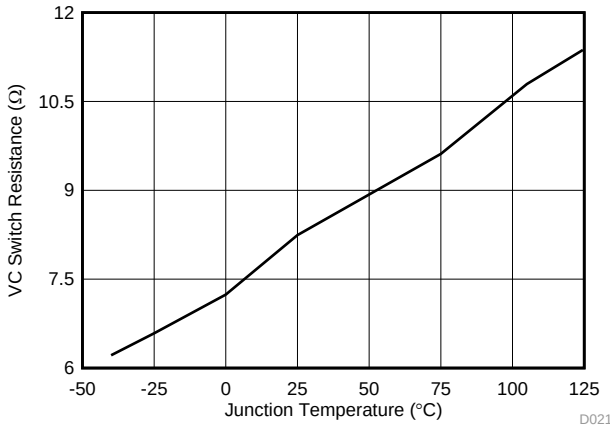


Figure 20. VC Switch Resistance vs Temperature

7 Detailed Description

7.1 Overview

The TPS2373 device is a 20-pin integrated circuit that contains all of the features needed to implement a single interface IEEE802.3bt Type-3 (TPS2373-3, -4) and Type-4 (TPS2373-4) powered device (PD). Basic functionality supported includes Detection, Hardware Classification, and inrush current limit (200-mA for TPS2373-3 and 335-mA for TPS2373-4) during startup. Enhanced features include the advanced startup function for DC-DC controller, as well as the automatic maintain power signature (MPS).

The TPS2373-3 integrates a low 0.3-Ω internal switch to support Type-3 applications up to 60 W of continuous power sourced by the PSE, allowing beyond 1.2 A (1.55 A minimum current limit) through the PD during normal operation.

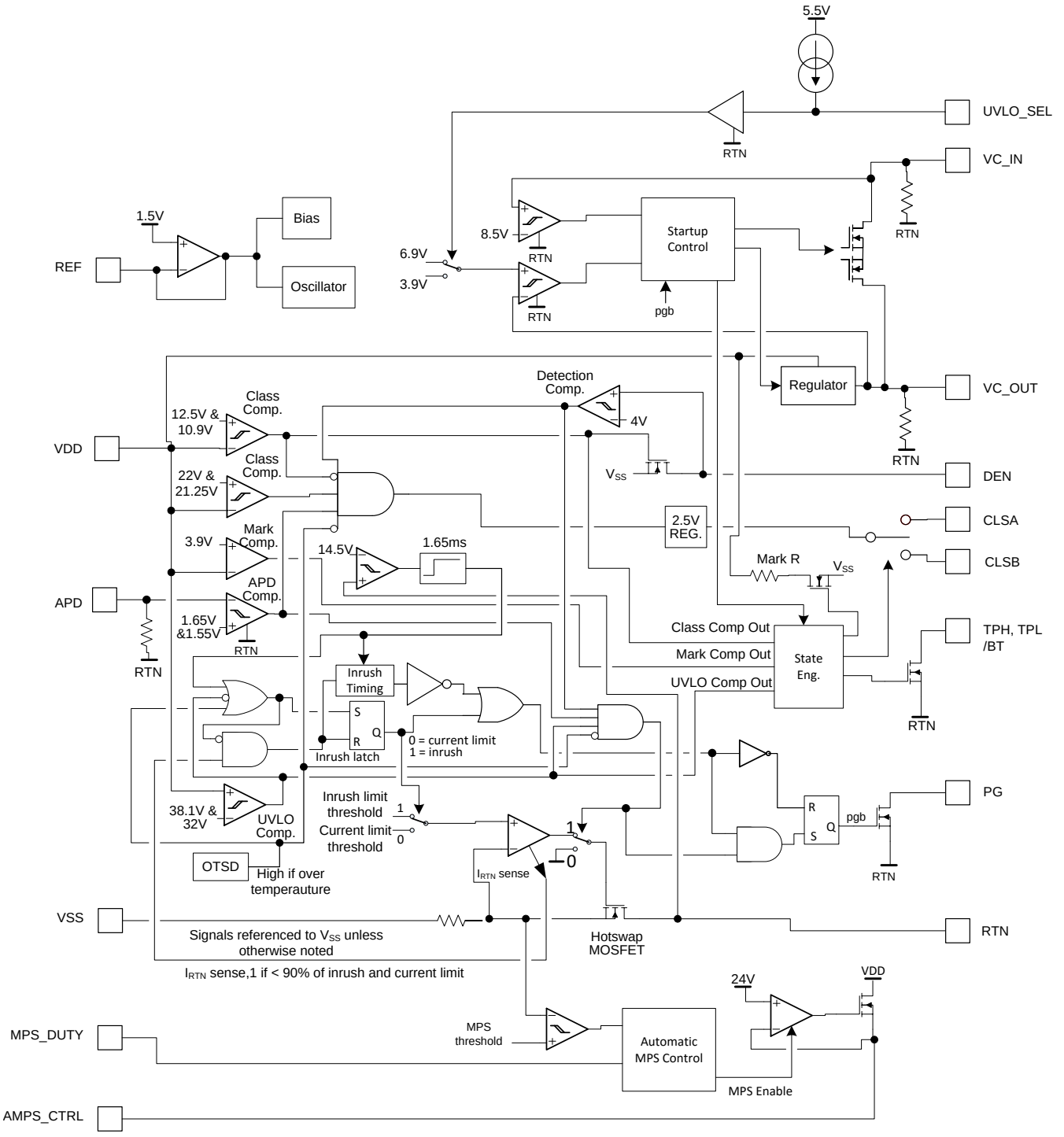
Likewise, the TPS2373-4 integrates a low 0.1-Ω internal switch to support Type-4 applications up to 90 W of continuous power sourced by the PSE, allowing up to 1.9 A through the PD during normal operation.

The TPS2373 has a built-in inrush time delay period, for a simple solution to meet the IEEE802.3bt startup requirement.

The TPS2373 features an auxiliary power detect (APD) input, providing priority for an external power adapter.

The TPS2373 contains several protection features such as thermal shutdown, current limit foldback, and a robust 100-V internal switch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 APD Auxiliary Power Detect

The APD pin is used in applications that may draw power either from the Ethernet cable or from an auxiliary power source. When a voltage of more than about 1.65 V is applied on the APD pin relative to RTN, the TPS2373 does the following:

- Internal pass MOSFET is turned off
- Classification current is disabled
- PG, TPL and $\overline{BT}$ outputs are forced to high impedance
- TPH output is turned on (low state)
- PWM startup is enabled without any inrush delay and over the full VDD voltage range, to allow operation from a low-voltage auxiliary power source
- The device will not properly detect due to PWM startup being enabled at low VDD voltage
- Maintain Power Signature (MPS) pulsed mode is enabled

This also gives adapter source priority over the PoE. A resistor divider (R_{APD1}–R_{APD2} in Figure 30) provides system-level ESD protection for the APD pin, discharges leakage from the blocking diode (D_A in Figure 30) and provides input voltage supervision to ensure that switch-over to the auxiliary voltage source does not occur at excessively low voltages. If not used, connect APD to RTN.

Note that R_{APD2} must be no more than 200 kΩ.

7.3.2 PG Power Good (Converter Enable) Pin Interface

PG is an active high output that is pulled to RTN when the device is in inrush phase. It remains in a high impedance state at all other times. This pin is an open-drain output, and it may require a pullup resistor or other interface to the downstream load. PG may be left open if it is not used.

The PG pin can be used to inhibit downstream converter startup by keeping the soft-start pin low. Figure 21 shows an example where PG connects to the SS pin of a DC-DC controller. Because PG is an open drain output, it will not affect the soft-start capacitor charge time when it deasserts. Another common use of the PG pin is to enable a converter with an active-high enable input. In this case, PG may require a pullup resistor to either VDD, or to a bias supply, depending on the requirements of the controller enable pin.

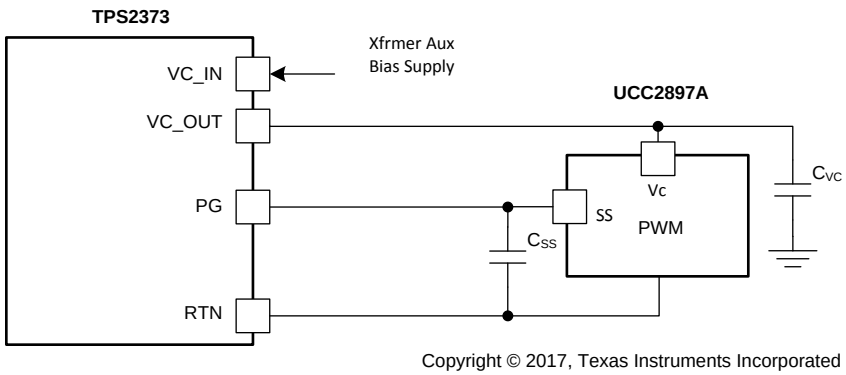


Figure 21. PG Interface

7.3.3 CLSA and CLSB Classification

Each of the two external resistors (R_{CLSA} and R_{CLSB} in Figure 30) connected between the CLSA (first and second class event) and CLSB (third and any subsequent class event) pins and VSS provide a distinct classification signature to the PSE, and are used to define the power class requested by the PD. The controller places a voltage of approximately 2.5 V across CLSA (first or second class event) or CLSB (all additional class events) external resistor whenever the voltage differential between VDD and VSS lies from about 10.9 V to 22 V. The current drawn by each resistor, combined with the internal current drain of the controller and any leakage through the internal pass MOSFET, creates the classification signature current. Table 1 lists the external resistor values

Feature Description (continued)

required for each of the PD power ranges defined by IEEE802.3bt. The number of classification cycles then determines how much power is allocated by the PSE. The maximum average power drawn by the PD, plus the power supplied to the downstream load, should not exceed the maximum power indicated in Table 1, as well as the maximum power allocated by the PSE based on the number of classification cycles. Holding APD high disables the classification signatures.

Type 2 and Type 3 PSEs may perform two classification cycles if Class 4 signature is presented on the first cycle. Likewise, Type 3 and Type 4 PSEs may perform four classification cycles if Class 4 signature is presented on the first two cycles and Class 0 or 1 signature is presented on the third cycle. Also, Type 4 PSEs may perform five classification cycles if Class 4 signature is presented on the first two cycles and Class 2 or 3 signature is presented on the third cycle.

Table 1. Class Resistor Selection

PD Class	CLASS SIGNATURE A	CLASS SIGNATURE B	MINIMUM POWER AT PD (W)	MAXIMUM POWER AT PD (W)	NUMBER OF CLASS CYCLES @ MAX POWER	RESISTOR CLSA (Ω)	RESISTOR CLSB (Ω)
0	0	0	0.44	12.95	1	1210	1210
1	1	1	0.44	3.84	1	249	249
2	2	2	3.84	6.49	1	140	140
3	3	3	6.49	12.95	1	90.9	90.9
4	4	4	12.95	25.5	2,3	63.4	63.4
5	4	0	25.5	40	4	63.4	1210
6	4	1	40	51	4	63.4	249
7	4	2	51	62	5	63.4	140
8	4	3	62	71	5	63.4	90.9

7.3.4 DEN Detection and Enable

DEN pin implements two separate functions. A resistor (R_{DEN} in Figure 30) connected between VDD and DEN generates a detection signature whenever the voltage differential between VDD and VSS lies from approximately 1.4 to 10.9 V. Beyond this range, the controller disconnects this resistor to save power. The IEEE 802.3bt standard specifies a detection signature resistance, R_{DEN} from 23.75 kΩ to 26.25 kΩ, or 25 kΩ ± 5%. TI recommends a resistor of 24.9 kΩ ± 1% for R_{DEN}.

Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET and class regulator to turn off. If the resistance connected between VDD and DEN is divided into two roughly equal portions, then the application circuit can disable the PD by grounding the tap point between the two resistances, while simultaneously spoiling the detection signature which prevents the PD from properly re-detecting.

7.3.5 Internal Pass MOSFET

RTN pin provides the negative power return path for the load. Once V_{VDD} exceeds the UVLO threshold, the internal pass MOSFET pulls RTN to VSS. Inrush limiting prevents the RTN current from exceeding a nominal value of about 200 mA and 335 mA for the TPS2373-3 and TPS2373-4 respectively until the bulk capacitance (C_{BULK} in Figure 30) is fully charged. Two conditions must be met to reach the end of inrush phase. The first one is when the RTN current drops below about 90% of nominal inrush current at which point the current limit is changed to 1.8 A for TPS2373-3 and 2.2 A for TPS2373-4, while the second one is to ensure a minimum inrush delay period of ~81.5 ms (t_{INR_DEL}) from beginning of the inrush phase. The PG output becomes high impedance to signal the downstream load that the bulk capacitance is fully charged and the inrush period has been completed.

If RTN ever exceeds about 14.5 V for longer than ~1.65 ms, then the TPS2373 returns to inrush phase; note that in this particular case, the second condition described above about inrush phase duration (81.5 ms) is not applicable.

7.3.6 TPH, TPL and $\overline{BT}$ PSE Type Indicators

The state of $\overline{BT}$, TPH and TPL is used to provide information relative to the PSE Type (1-2 or 3-4) and its allocated power. Table 2 lists the encoding corresponding to various combinations of PSE Type, PD Class and allocated power. Table 3 also corresponds to cases where the PSE allocated power is lower than what the PD is requesting. The allocated power is determined by the number of classification cycles having been received. During startup, the TPH, TPL and $\overline{BT}$ outputs are enabled typically 24 ms after V_{VC_IN} went high, to allow the power supply to reach a stable state first. In applications where VC_IN is tied to a DC voltage already present before end of inrush, the 24-ms delay applies from when PG output went from low to open state. These 3 outputs will return to a high-impedance state if the part enters thermal shutdown, if VC_OUT voltage falls below its UVLO threshold, or if VDD-to-VSS voltage falls below ~32 V. Note that in all these cases, as long as VDD-to-VSS voltage remains above the mark reset threshold, the internal logic state of these 3 signals is remembered such that these outputs will be activated accordingly after the startup has completed. This circuit resets when the VDD-to-VSS voltage drops below the mark reset threshold. The TPH, TPL and $\overline{BT}$ pins can be left unconnected if not used.

Table 2. TPH, TPL, $\overline{BT}$ and Allocated Power Truth Table

PSE Type	PD Class	NUMBER OF CLASS CYCLES	PSE ALLOCATED POWER AT PD (W)	TPH	TPL	$\overline{BT}$
1-2	0	1	12.95	HIGH	HIGH	HIGH
1-2	1	1	3.84	HIGH	HIGH	HIGH
1-2	2	1	6.49	HIGH	HIGH	HIGH
1-2	3	1	12.95	HIGH	HIGH	HIGH
2	4	2	25.5	HIGH	LOW	HIGH
3-4	0	1	12.95	HIGH	HIGH	LOW
3-4	1	1	3.84	HIGH	HIGH	LOW
3-4	2	1	6.49	HIGH	HIGH	LOW
3-4	3	1	12.95	HIGH	HIGH	LOW
3-4	4	2-3	25.5	HIGH	LOW	LOW
3-4	5	4	40	LOW	HIGH	LOW
3-4	6	4	51	LOW	HIGH	LOW
4	7	5	62	LOW	LOW	LOW
4	8	5	71	LOW	LOW	LOW

Table 3. Power Demotion Cases

PSE Type	PD Class	NUMBER OF CLASS CYCLES	PSE ALLOCATED POWER AT PD (W)	TPH	TPL	$\overline{BT}$
3-4	4-8	1	12.95	HIGH	HIGH	LOW
3-4	5-8	2,3	25.5	HIGH	LOW	LOW
3-4	7-8	4	51	LOW	HIGH	LOW

7.3.7 VC_IN, VC_OUT, UVLO_SEL and Advanced PWM Startup

VC_OUT provides the auxiliary power supply for the external DC-DC controller. After the inrush phase has completed, VC_OUT initially sources the startup current from VDD input, then it is internally connected to VC_IN once V_{VC_IN} has exceeded approximately 8.5 V, meaning that the DC-DC converter has ramped up its output voltage, or if V_{VC_IN} has remained below 8.5 V for more than about 50 ms (time out period). VC_IN is usually fed by a bias winding of the DC-DC converter's power transformer to sustain operation after startup. The startup current source is turned on at the end of the inrush phase, and it is turned off about 24 ms after the VC switch, connecting VC_IN and VC_OUT together, has been turned on. Due to the high current capability of the startup source, the recommended capacitance at VC_OUT is relatively small, typically 1 µF in most applications, including when there is auxiliary power input in the range of 20V and higher. VC_IN capacitance is also typically 1/10 of VC_OUT capacitance to avoid a significant voltage drop at VC_OUT when the VC switch is turned on.

Once V_{VC_OUT} falls below its UVLO threshold, the startup current source is turned back on, while the VC switch is turned off, initiating a new PWM startup cycle. The UVLO_SEL input is used to select the VC_OUT UVLO threshold between ~6.9 V and ~3.9 V, which should be slightly below the minimum falling UVLO threshold of the PWM controller.

If VC_OUT is not used, VC_IN must be connected to the low voltage bias supply of the PWM controller to ensure proper operation.

7.3.8 AMPS_CTL, MPS_DUTY and Automatic MPS

To maintain PSE power, the AMPS_CTL output generates voltage pulses. This is translated into current pulses by connecting a resistor between AMPS_CTL and VSS. These pulses are automatically generated as long as the current through the RTN-to-VSS path is not high enough (< ~28 mA). Typical resistor value of 1.3 kΩ is recommended, in applications where the load current may go below ~20 mA and the PSE power has to be maintained.

If a Type 3 or 4 PSE is detected, the MPS_DUTY input can be used to select one out of three duty-cycles (5.4%, 8.1%, 12.5%). The selection is based on various system parameters, which include the amount of bulk capacitance, the input cable impedance and the type of input bridge. Also, inserting a blocking diode (or MOSFET) between the bulk capacitor and the TPS2373 allows the selection of a shorter MPS duty-cycle.Table 4 should be used to select a proper MPS Duty Cycle.

Table 4. MPS Duty-Cycle Selection

PSE Type	MPS_DUTY	MPS Duty-Cycle
1,2	-	26%
3,4	Short to VSS	12.5%
3,4	Resistance (60.4K typ.) to VSS	8.1%
3,4	Open	5.4%

Table 5. System Conditions and MPS Duty-Cycle

Expected PoE PD System Conditions			MPS_DUTY Selection		
C_{BULK} Blocking Diode	C_{BULK}	Cable Length	MPS Duty-cycle	Pin Termination	I_{MPS} (mA)
Yes	Any	0 -100m	5.4% or longer	Open	18.5
No	≤ 60 µF		8.1% or longer	60 kΩ to VSS	18.5
No	> 60 µF, ≤ 120 µF		12.5%	Short to VSS	18.5
No	≤ 120 µF		5.4% or longer(1)	Open	18.5
No	> 120 µF, ≤ 300 µF		8.1% or longer (1)	60 kΩ to VSS	18.5

(1) Applicable when PSE voltage step-down events are unlikely or are not expected to exceed -0.4 V.

7.3.9 VDD Supply Voltage

VDD pin connects to the positive side of the input supply. It provides operating power to the PD controller and allows monitoring of the input line voltage. If V_{VDD} falls below its UVLO threshold and goes back above it, or if a thermal shutdown resumes while V_{VDD} is already above its UVLO threshold, the TPS2373 returns to inrush phase.

7.3.10 VSS

VSS pin is the input supply negative rail that serves as a local ground. The exposed thermal PAD must be connected to this pin to ensure proper operation.

7.3.11 Exposed Thermal PAD

The exposed thermal PAD is internally connected to VSS pin. It should be tied to a large VSS copper area on the PCB to provide a low resistance thermal path to the circuit board. TI recommends maintaining a clearance of 0.025” between VSS and high-voltage signals such as VDD.

7.4 Device Functional Modes

7.4.1 PoE Overview

The following text is intended as an aid in understanding the operation of the TPS2373 but not as a substitute for the IEEE 802.3bt standard. The pending IEEE 802.3bt standard is an update to IEEE 802.3-2012 clause 33 (PoE), adding 4-pair power, high-power options, additional features and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2012 is referred to as a Type 1 (Class 0-3) or 2 (Class 4) device, and devices with higher power and enhanced classification will be referred to as Type 3 (Class 5,6) or 4 (Class 7,8) devices. Type 3 devices will also include Class 0-4 devices that are 4-pair capable. Standards change and should always be referenced when making design decisions.

The IEEE 802.3bt standard defines a method of safely powering a PD (powered device) over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. There is also a fourth operational state used by Type 3 and 4 PSEs, called "connection check", to determine if the PD has same (single interface) or independent (dual interface or commonly referred to "dual-signature" in the IEEE802.3bt standard) classification signature on each pairset. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection, and also includes connection check if Type 3 or 4 PSE. The low power levels used during detection and connection check are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Type 3 or Type 4 PSEs are required to do an enhanced hardware classification of Type 3 or 4 respectively. Type 2 PSEs are required to do Type 1 hardware classification plus a data-layer classification, or an enhanced Type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A Type 3 or Type 4 PD must do respectively Type 3 or Type 4 hardware classification as well as DLL classification. A Type 2 PD must do Type 2 hardware classification as well as DLL classification. The PD may return the default, 13-W current-encoded class, or one of four other choices if Type 2, one of six other choices if Type 3, and one of eight other choices if Type 4. DLL classification occurs after power-on and the Ethernet data link has been established.

Once started, the PD must present a maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 22 shows the operational states as a function of PD input voltage.

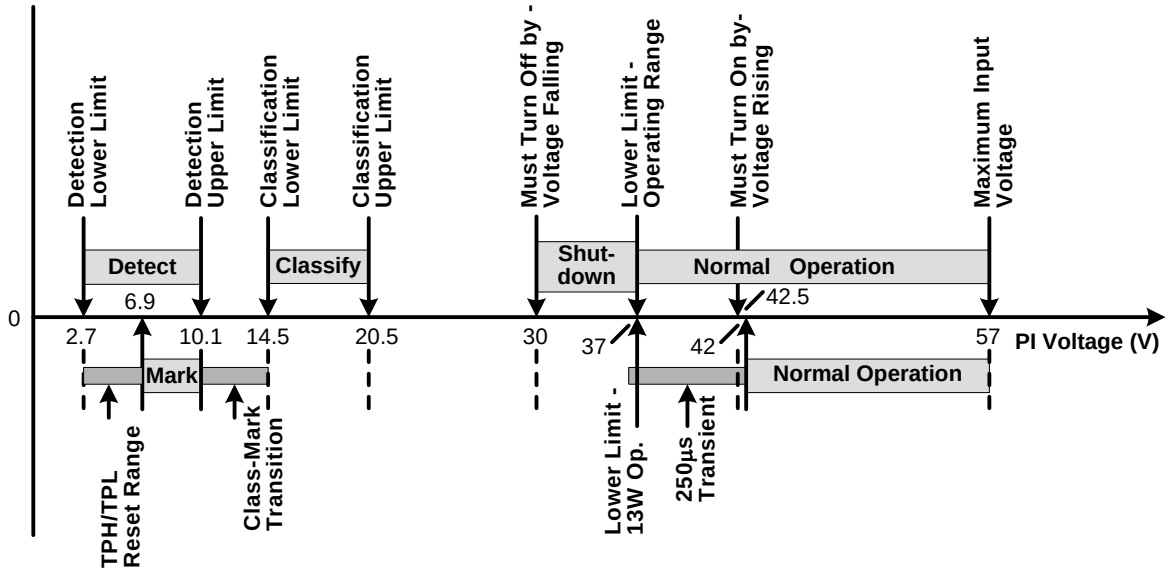


Figure 22. Operational States

Device Functional Modes (continued)

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2008 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at Type 2 and IEEE 802.3bt Type 3 cabling power loss allotments and voltage drops have been adjusted for 12.5-Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG 24 conductors). Table 6 shows key operational limits broken out for the two revisions of the standard.

Table 6. Comparison of Operational Limits

STANDARD	POWER LOOP RESISTANCE (MAX)	PSE OUTPUT POWER (MIN)	PSE STATIC OUTPUT VOLTAGE (MIN)	PD INPUT POWER (MAX)	STATIC PD INPUT VOLTAGE	
					POWER ≤ 13 W	POWER > 13 W
IEEE802.3-2012 802.3at (Type 1)	20 Ω	15.4 W	44 V	13 W	37 V – 57 V	N/A
802.3bt (Type 3)	12.5 Ω		50 V			
802.3at (Type 2) 802.3bt (Type 3)	12.5 Ω	30 W	50 V	25.5 W	37 V – 57 V	42.5 V – 57 V
802.3bt (Type 3)	6.25 Ω (4-pair)	60 W	50 V	51 W	N/A	42.5 V - 57 V
802.3bt (Type 4)	6.25 Ω (4-pair)	90 W	52 V	71.3 W	N/A	41.2 V - 57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6 for 10baseT or 100baseT), or between the two spare pairs (4–5 and 7–8). Power application to the same pin combinations in 1000/2.5G/5G/10GbaseT systems is recognized in IEEE 802.3bt. 1000/2.5G/5G/10GbaseT systems can handle data on all pairs, eliminating the spare pair terminology. Type 1 and 2 PSEs are allowed to apply voltage to only one set of pairs at a time, while Type 3 and 4 PSEs may apply power to one or both sets of pairs at a time. The PD uses input diode or active bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS2373 specifications.

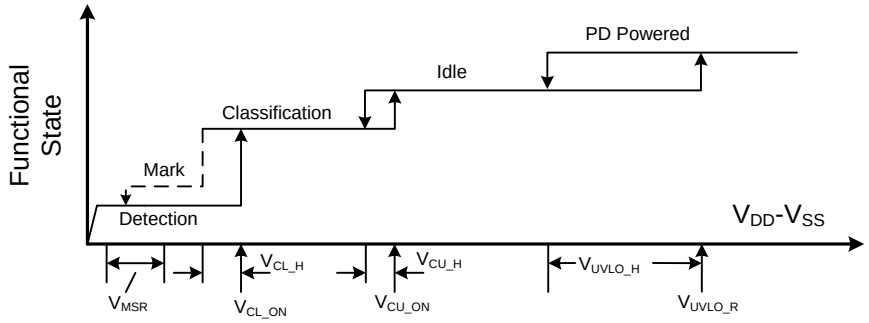
A compliant Type 2, 3 or 4 PD has power management requirements not present with a Type 1 PD. These requirements include the following:

1. Must interpret respectively Type 2, 3 or 4 hardware classification.
2. Must present hardware Class 4 during the first two classfication events, applicable to Type 2 and 4 PDs, as well as to Type 3 PD with Class level 4 or higher.
3. If Type 3 or 4 single interface PD, it must present hardware Class in the range of 0 to 3 during the third and any subsequent classification events.
4. Must implement DLL negotiation.
5. Must behave like a Type 1 PD for 50 ms then must draw less than 400 mA until 80 m after the PSE applies operation voltage (power up), if Type 2 or 3 single interface PD. This covers the PSE inrush period, which is 75 ms maximum.
6. Should behave like a Type 1 PD for 50 ms then must draw less than 400 mA until 80 ms after the PSE applies operation voltage (power up), if Type 4 single interface PD.
7. Must not draw more than 60 mA and 5 mA any time the input voltage falls below respectively 30 V and 10 V.
8. Must not draw more than 13 W if it has not received at least a Type 2 hardware classification or received permission through DLL.
9. Must not draw more than 25.5 W if it has not received at least 4 classification events or received permission through DLL.
10. Must not draw more than 51 W if it has not received at least 5 classification events or received permission through DLL.
11. Must meet various operating and transient templates.
12. Optionally monitor for the presence or absence of an adapter (assume high power).

As a result of these requirements, the PD must be able to dynamically control its loading, and monitor TPL and TPH for changes. In cases where the design needs to know specifically if an adapter is plugged in and operational, the adapter should be individually monitored, typically with an optocoupler.

7.4.2 Threshold Voltages

The TPS2373 has a number of internal comparators with hysteresis for stable switching between the various states. Figure 23 relates the parameters in *Electrical Characteristics* to the PoE states. The mode labeled Idle between Classification and Operation implies that the DEN, CLSA, CLSB, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the Type 2-3-4 hardware class state machine.



Note: Variable names refer to Electrical Characteristic Table parameters

Figure 23. Threshold Voltages

7.4.3 PoE Startup Sequence

The waveforms of Figure 24 demonstrate detection, classification , and startup from a PSE with Type 3 Class 6 hardware classification. The key waveforms shown are $V_{(VDD-VSS)}$, $V_{(RTN-VSS)}$ and I_{PI}. IEEE 802.3bt requires a PSE allocating Class 6 level of power to generate a minimum of two detection levels, four class and mark cycles, and startup from the fourth mark event. As shown below, the required minimum duration of the first class event has been extended for Type 3 and 4 PSEs. V_{RTN} to V_{SS} falls as the TPS2373 charges C_{BULK} following application of full voltage. In Figure 26, assertion of the PG signal is delayed and used to enable load current as seen in the I_{PI} waveform.

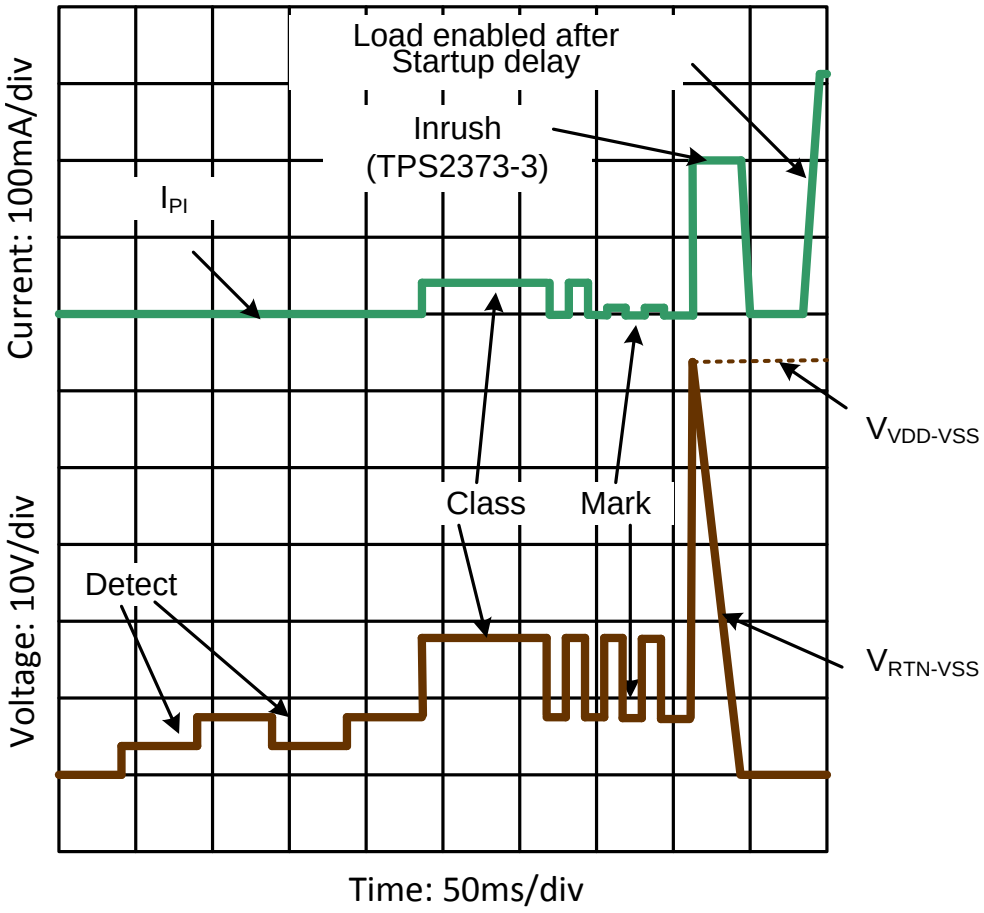


Figure 24. Startup of Class 6 PD

7.4.4 Detection

The TPS2373 pulls DEN to V_{SS} whenever $V_{(VDD-VSS)}$ is below the lower classification threshold. When the input voltage rises above V_{CL_ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DEN} of 24.9 kΩ (±1%), presents the correct signature. It may be a small, low-power resistor because it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance ($\Delta V / \Delta I$) from 23.7 kΩ to 26.3 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and internal V_{DD} loading. The input diode bridge's incremental resistance may be hundreds of Ω at the low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially compensated by the TPS2373 effective resistance during detection.

The hardware classification protocol of IEEE 802.3bt specifies that a Type 2, 3 or 4 PSE drops its output voltage into the detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as a mark event (see Figure 24). After the first mark event, the TPS2373 will present a signature less than 12 kΩ until it has experienced a $V_{(VDD-VSS)}$ voltage below the mark reset threshold (V_{MSR}). This is explained more fully under *Hardware Classification*.

7.4.5 Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before powering, and helps with power management once power is applied. Type 2, 3, and 4 hardware classification permits high power PDs to determine whether the PSE can support its high-power operation. The number of class cycles generated by the PSE prior to turn on indicates to the PD if it allots the power requested or if the allocated power is less than requested, in which case there is power demotion as shown in Table 3. A Type 2 PD always presents Class 4 in hardware to indicate that it is a 25.5W device. A Class 5 or 6 Type 3 PD presents Class 4 in hardware during the

first two class events and it presents Class 0 or 1, respectively, for all subsequent class events. A Class 7 or 8 Type 4 PD presents Class 4 in hardware during the first two class events and it presents Class 2 or 3, respectively, for all subsequent class events. A Type 1 PSE will treat a Class 4 to 8 device like a Class 0 device, allotting 13 W if it chooses to power the PD. A Type 2 PSE will treat a Class 5 to 8 device like a Class 4 device, allotting 25.5W if it chooses to power the PD. A Class 4 PD that receives a 2-event class, a Class 5 or 6 PD that receives a 4-event class, or a Class 7 or 8 PD that receives a 5-event class, understands that the PSE has agreed to allocate the PD requested power. In the case where there is power demotion, the PD may choose to not start, or to start while not drawing more power than initially allocated, and request more power through the DLL after startup. The standard requires a Type 2, 3 or 4 PD to indicate that it is underpowered if this occurs. Startup of a high-power PD at lower power than requested implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in Table 1 determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated class power, which may be the hardware class or a DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the Table 1 limit; however, the average power requirement always applies.

The TPS2373 implements one- to five-event classification. R_{CLSA} and R_{CLSB} resistor values define the class of the PD. DLL communication is implemented by the Ethernet communication system in the PD and is not implemented by the TPS2373.

The TPS2373 disables classification above V_{CU_ON} to avoid excessive power dissipation. CLSA/B voltage is turned off during PD thermal limiting or when APD or DEN is active. The CLSA and CLSB outputs are inherently current-limited, but should not be shorted to V_{SS} for long periods of time.

Figure 25 shows how classification works for the TPS2373. Transition from state-to-state occurs when comparator thresholds are crossed (see Figure 22 and Figure 23). These comparators have hysteresis, which adds inherent memory to the machine. Operation begins at idle (unpowered by PSE) and proceeds with increasing voltage from left to right. A 2- to 5-event classification follows the (heavy lined) path towards the bottom, ending up with a latched TPL/TPH decode along the lower branch that is highlighted. Once the valid path to the PSE detection is broken, the input voltage must transition below the mark reset threshold to start anew.

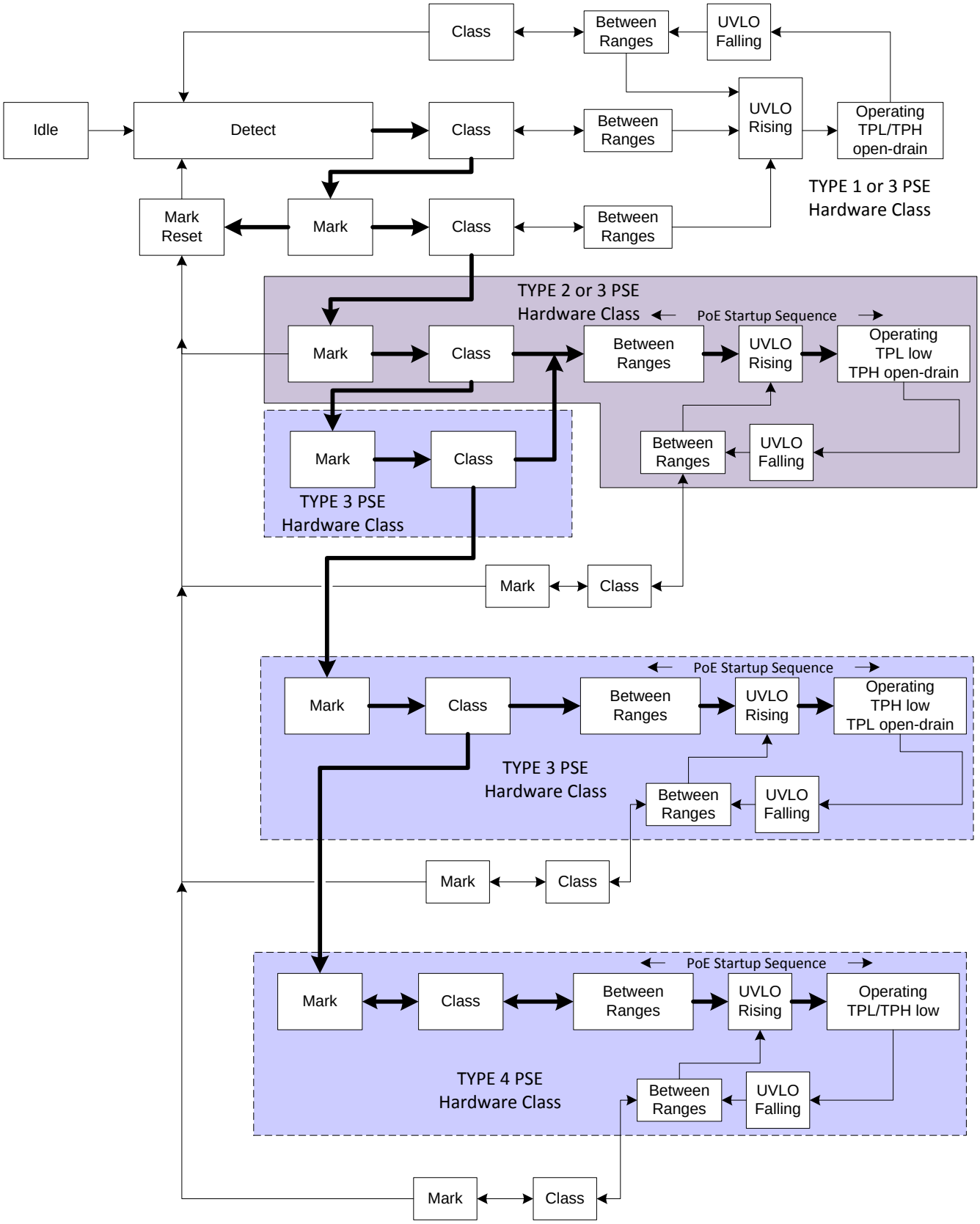


Figure 25. Up to Five-Event Class Internal States

7.4.6 Inrush and Startup

IEEE 802.3bt has a startup current and time limitation, providing compatibility between a PSE of any Type and a PD of any Type. The PSE inrush limit varies according to the allotted power. If Class 0 to 4, Class 5 to 6 or Class 7 to 8, the inrush limit is respectively from 400 mA to 450 mA, 400 mA to 900 mA or 800 mA to 900 mA. PSE inrush limit applies for up to 75 ms after power up (applying "48 V" to the PI), after which the Type 2, 3, or 4 PSE will support a higher output current in accordance with the allocated class. The TPS2373-3 and TPS2373-4 respectively implement a 200-mA and 335-mA inrush current, which is compatible with all PSE Types. A high-power PD must limit its converter startup peak current. The operational current for Type 2 and 3, and preferably Type 4, cannot exceed 400 mA for a period of 80 ms.

7.4.7 Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. For a Type 1 or Type 2 PD, a valid MPS consists of a minimum dc current of 10 mA, or a 10-mA pulsed current for at least 75 ms every 325 ms, and an AC impedance lower than 26.3 kΩ in parallel with 0.05 μF. Only Type 1 and Type 2 PSEs monitor the AC MPS. A Type 1 or Type 2 PSE that monitors only the AC MPS may remove power from the PD.

To enable applications with stringent standby requirements, IEEE802.3bt introduced a significant change regarding the minimum pulsed current duration to assure the PSE will maintain power. This applies to all Type 3 and Type 4 PSEs, and the pulse duration is ~10% of what is required for Type 1 and 2 PSEs. The MPS current amplitude requirement for Class 5-8 PDs have also increased to 16 mA at the PSE end of the ethernet cable.

If the current through the RTN-to-VSS path is below ~28 mA, the TPS2373 automatically generates the MPS pulsed current through the AMPS_CTL output pin, the current amplitude being adjustable with an external resistor. The TPS2373 is also able to determine if the PSE is of Type 1-2 or Type 3-4, automatically adjusting the MPS pulse duration and duty-cycle. Note that the IEEE802.3bt requirement for the PD is applicable at the PSE end of the cable. That means that depending the cable length and other parameters including the bulk capacitance, a longer MPS duration may be required to ensure a valid MPS. For that purpose, the TPS2373 has 3 different selections of MPS pulse duration and duty-cycle, selectable through the MPS_DUTY input pin. Note that the MPS pulsed mode also applies when APD is pulled high.

When DEN is used to force the hotswap switch off, the DC MPS will not be met. A PSE that monitors the DC MPS will remove power from the PD when this occurs.

7.4.8 Advanced Startup and Converter Operation

The internal PoE UVLO (Undervoltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the downstream converter circuits from loading the PoE input during detection and classification. The converter circuits will discharge C_{BULK} while the PD is unpowered. Thus $V_{(VDD-RTN)}$ will be a small voltage just after full voltage is applied to the PD, as seen in Figure 24. The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{VDD} rises above the UVLO turn-on threshold (V_{UVLO_R}, approximately 38 V) with RTN high, the TPS2373-3 and TPS2373-4 enables the hotswap MOSFET with inrush current limit (~200 mA for TPS2373-3 and ~335 mA for TPS2373-4) as seen in Figure 26. The PG pin is in low state while C_{BULK} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}. VC_OUT output is also turned off during that time, providing no low supply voltage to the PWM controller, to avoid additional loading between V_{VDD} and V_{RTN} that could prevent successful PD and subsequent converter start up. Once the inrush current falls about 10% below the inrush current limit, the PD current limit switches to the operational level (~1.8 A for TPS2373-3 and ~2.2 A for TPS2373-4).

Additionally, as seen in Figure 26 once the inrush period duration has also exceeded ~81.5 ms, PG output becomes high impedance and the PWM controller startup source is turned on charging C_{VC_OUT}, the VC_OUT capacitor, and allowing the downstream converter circuitry to start. As seen in Figure 27, the converter soft-start introduces a slight additional delay before the start of switching. Note that the startup source current capability is such that it can fully maintain V_{VC_OUT} during the converter soft-start without requiring any significant C_{VC_OUT} capacitance. Once V_{VC_IN} has risen above V_{VCIN_ON} (~8.5 V), meaning that the DC-DC converter has ramped up its output voltage, VC_IN pin is internally connected to VC_OUT pin. The startup current source is then turned off ~24 ms (t_{TPLHBT}) later, completing the startup. TPH, TPL and $\overline{BT}$ outputs are enabled within t_{TPLHBT} following V_{VC_IN} rising above V_{VCIN_ON}. If there is a fault condition preventing V_{VC_IN} from rising during converter startup (for example a short-circuit at the output of the downstream converter), a t_{STUP_OUT} (~50 ms) timeout period is applied at the end of which the startup source is turned off and the VC switch is turned on, until V_{VC_OUT} falls below V_{VCO_UV} to initiate a new startup cycle.

The falling VC_OUT UVLO threshold (V_{VCO_UV}) needs to be below the minimum falling UVLO threshold of the PWM controller, to ensure that every time the TPS2373 initiates a new startup cycle, the PWM controller has already reached a reset state and will initiate a new soft-start sequence. V_{VCO_UV} is selectable between nominally 6.9 V and 3.9 V, via the UVLO_SEL input, to accommodate various PWM controllers.

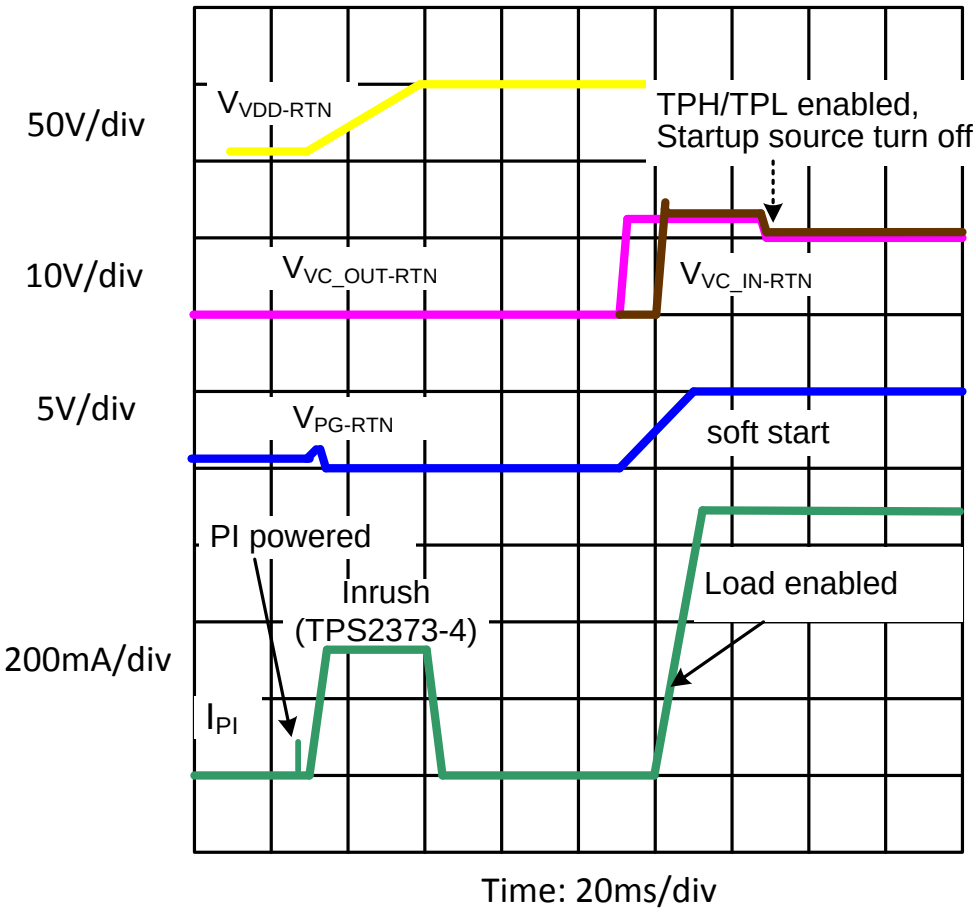


Figure 26. Power Up and Start

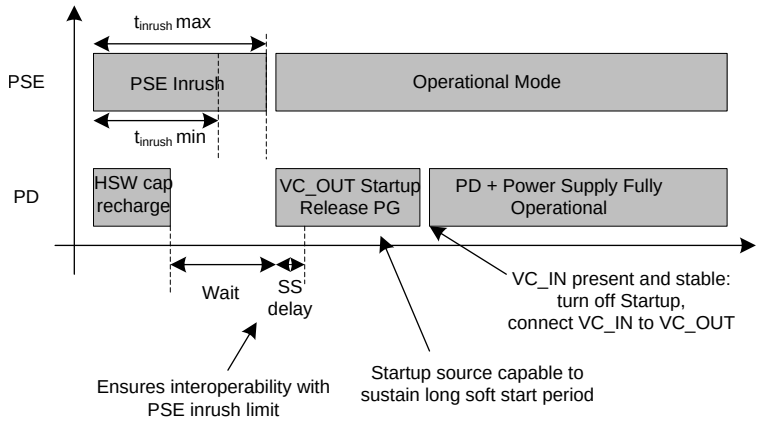


Figure 27. Power Up and Start

If V_{VDD}-V_{VSS} drops below the lower PoE UVLO (V_{UVLO_F}, ~32 V), the hotswap switch is turned off, but the PG output remains high impedance allowing the converter to continue operating until V_{VC_OUT} falls below the PWM controller's UVLO threshold.

7.4.9 PD Hotswap Operation

IEEE802.3bt includes new PSE output limiting requirements for Type 3 and 4 operation to cover higher power and 4-pair applications. Type 2, 3 and 4 PSEs must meet an output current vs time template with specified minimum and maximum sourcing boundaries. The peak output current per each 2-pair may be as high as 50 A for 10 μs or 1.75 A for 75 ms, and the total peak current becomes twice these values when power is delivered over 4 pairs. This makes robust protection of the PD device even more important than it was in IEEE 802.3-2012.

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with $V_{(RTN-VSS)}$ rising as a result. If $V_{(RTN-VSS)}$ rises above approximately 14.5 V for longer than approximately 1.65 ms, the current limit reverts to the inrush value and PG output is forced low which turns off the converter, although there is no minimum inrush delay period (81.5-ms) applicable in this case. The 1.65-ms deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 28 shows an example of the RTN current profile during V_{DD} to RTN short circuit, using 5-ohm load impedance. The hotswap MOSFET goes into current limit, causing the RTN voltage to increase. Once V_{RTN} exceeds 14.5 V, I_{RTN}, which was clamped to the current limit drops to the level of inrush current limit after 1.65 ms.

The inrush current limit is also reestablished when $V_{(VDD-VSS)}$ drops below UVLO then rises above it.

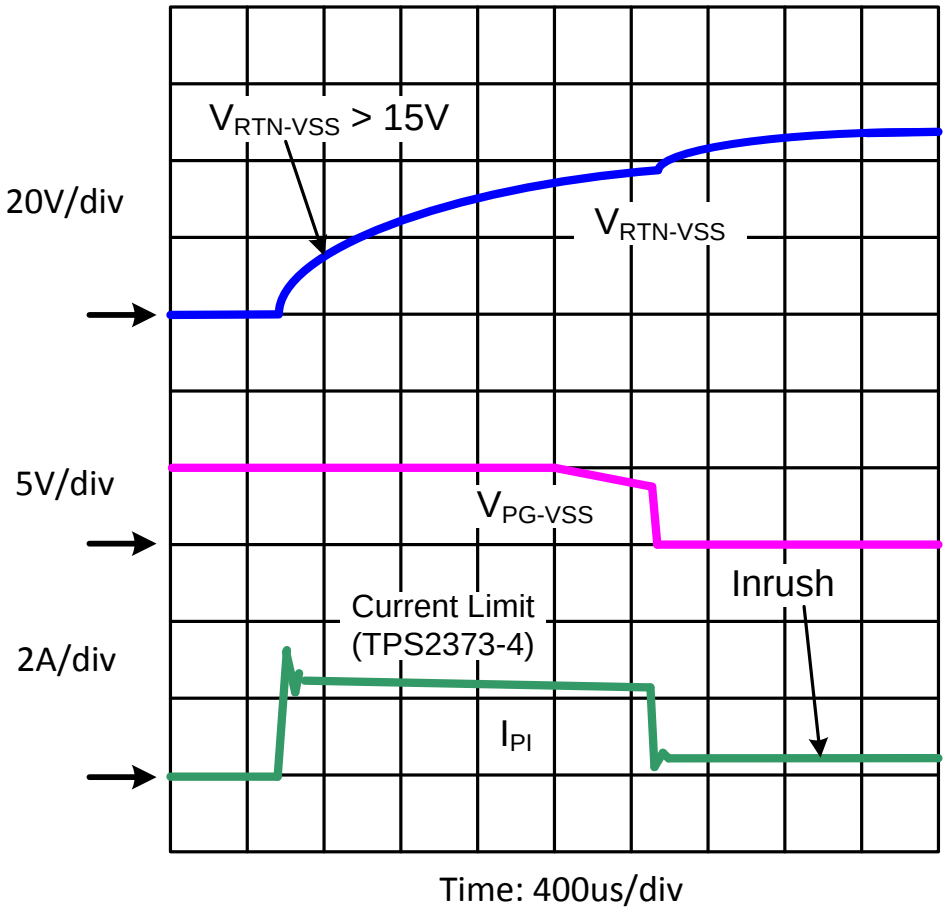


Figure 28. Response to PD Output Short Circuit

The PD control has thermal sensors that protect the internal hotswap MOSFET, the startup current source and the MPS pulsed current driver. Conditions like startup or operation into a V_{DD}-to-RTN short cause high power dissipation in the MOSFET. An over-temperature shutdown (OTSD) turns off the hotswap MOSFET, the class regulator, the startup current source, and the MPS driver, which are restarted after the device cools. The hotswap MOSFET will be re-enabled and the TPS2373 will return to inrush phase when exiting from an overtemperature event. Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with option three ORing per Figure 29 to achieve adapter priority.

The hotswap switch will be forced off under the following conditions:

1. V_{APD} above V_{APDEN} (approximately 1.65 V),
2. $V_{(DEN\ –VSS)} < V_{PD\text{-}DIS}$ when $V_{(VDD\text{-}VSS)}$ is in the operational range,
3. PD is over-temperature, or
4. $V_{(VDD\ –VSS)}$ < PoE UVLO falling threshold (approximately 32 V).

7.4.10 Startup and Power Management, PG and TPH, TPL, $\overline{BT}$

PG (power good or converter enable) is a pin that when at low level indicates when the internal hotswap MOSFET is in inrush phase. PG goes high impedance when inrush phase is over and can be used to enable a downstream converter to start up. Common interfaces to the converter controller include the soft-start or enable pins.

TPH, TPL and $\overline{BT}$ provide information relative to the PSE Type (1-2 or 3-4) and its allocated power. It can also indicate if the APD is driven high, in which case the code becomes "Low-High-High", respectively.

Using the APD encoding allows the PD to operate from an adapter at high-power if a PSE with enough power capability is not present, assuming the adapter has sufficient capacity. Applications must monitor the state of TPH, TPL and $\overline{BT}$ to detect power source transitions. Transitions could occur when a local power supply is added or dropped, or when a PSE is enabled on the far end. The PD may be required to adjust the load appropriately. The usage of TPH/TPL/$\overline{BT}$ is demonstrated in Figure 30.

The TPS2373 is also able to interoperate with non standard PoE++ PSE controllers. If powered from a PoE++ PSE controller, the TPH/TPL/$\overline{BT}$ 3-bit code becomes "Low-Low-High". This also indicates that the PoE++PSE agreed to deliver the power requested by the TPS2373.

7.4.11 Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS2373 supports forced operation from either of the power sources. Figure 29 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS2373 PoE input, option 2 applies power between the TPS2373 PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. Many of the basic ORing configurations and much of the discussion contained in the application note *Advanced Adapter ORing Solutions* using the TPS23753 (SLVA306), apply to the TPS2373 incorporating a DC/DC converter.

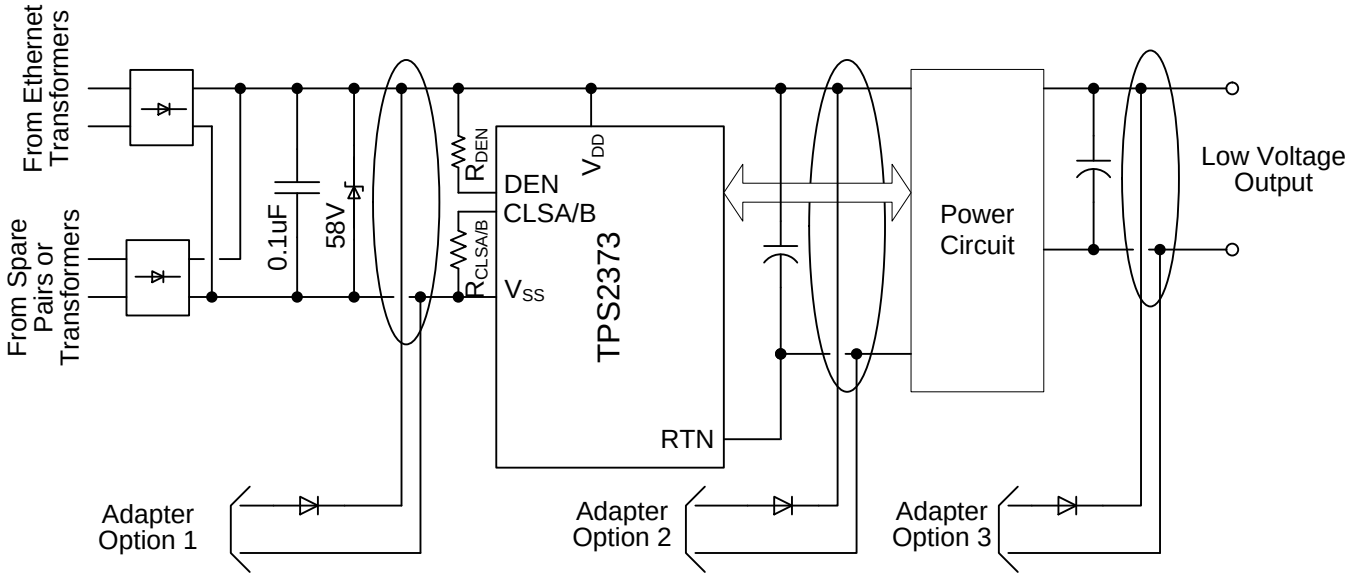


Figure 29. Oring Configurations

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for ORing options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, or damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

7.4.12 Using DEN to Disable PoE

The DEN pin may be used to turn the PoE hotswap switch off by pulling it to V_{SS} while in the operational state, or to prevent detection when in the idle state. A low voltage on DEN forces the hotswap MOSFET off during normal operation. Additional information is available in the *Advanced Adapter ORing Solutions* using the TPS23753 (SLVA306) application report.

7.4.13 ORing Challenges

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors adding to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult, if not impossible, for many of the combinations. However, the TPS2373 offers several built-in features that simplify some combinations.

Several examples demonstrate the limitations inherent in ORing solutions. Diode ORing a 48-V adapter with PoE (option 1) presents the problem that either source may have the higher voltage. A blocking switch would be required to assure that one source dominates. A second example combines a 12-V adapter with PoE using option 2. The converter draws approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from PoE power to adapter may demand more current than can be supplied by the PSE. The converter must be turned off while the C_{BULK} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS2373 has the flexibility to be implemented in IEEE802.3bt and PoE++ PDs. Therefore, it can be used in a wide range applications such as video and VoIP telephones, multiband access points, security cameras, and pico-base stations.

8.2 Typical Application

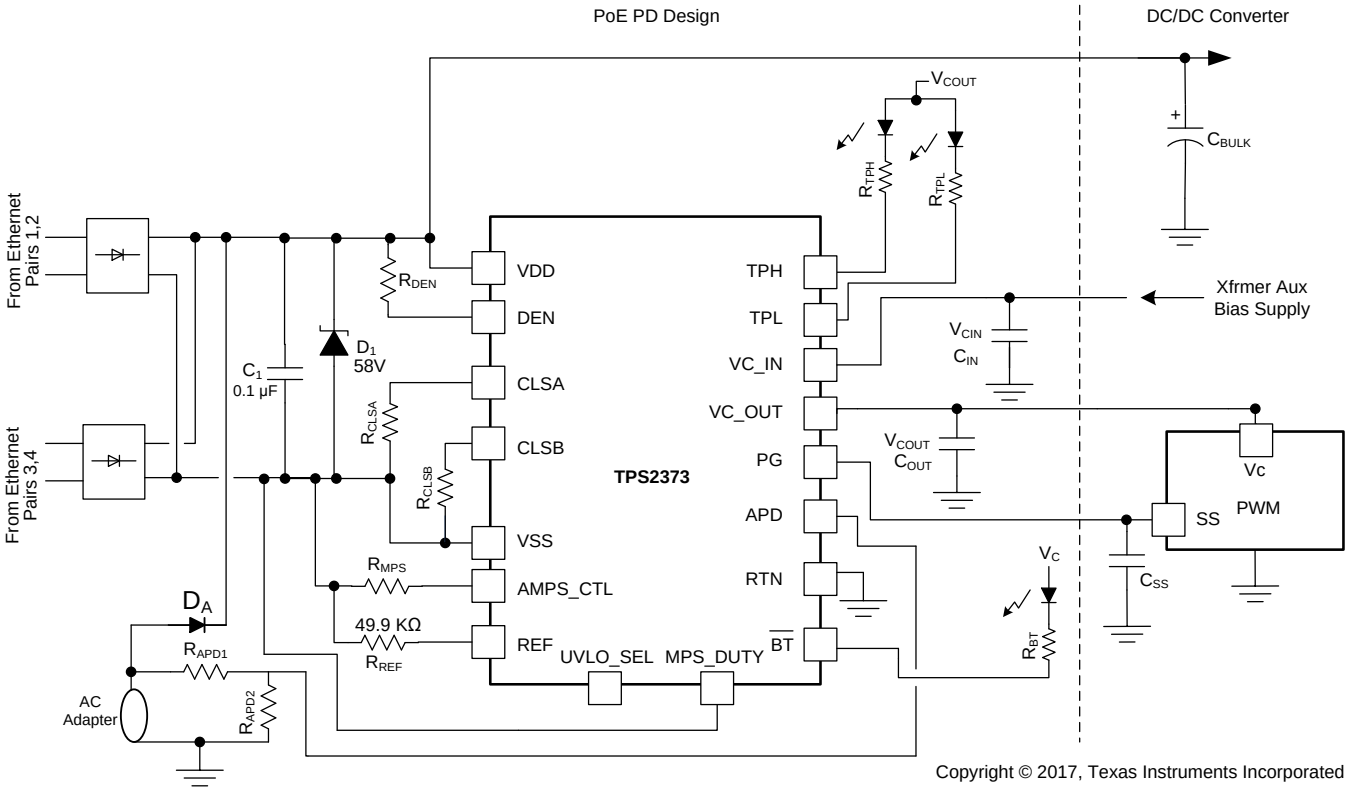


Figure 30. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters in Table 7 for a PD Class 8 application.

Table 7. Design Parameters

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
POWER INTERFACE				
Input voltage	Power applied through PoE or adapter	0	57	V
Operating voltage	After startup	30	57	V
Adapter voltage		40	57	V
Input UVLO	Rising input voltage at device terminals	—	40	V
	Falling input voltage	30.5	—	
Detection voltage	At device terminals	1.4	10.1	V
Classification voltage	At device terminals	11.9	23	V
PD class 8	Class signature A	38	42	mA
PD class 8	Class signature B	26.5	29.3	mA
Inrush current limit		275	395	mA
Operating curent-limit		1.9	2.5	A
PWM controller	UCC2897A			
Automatic MPS	12.5% Duty Cycle at no load			

8.2.2 Detailed Design Requirements

8.2.2.1 Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges will reduce the power dissipation in these devices by about 30%. There are, however, some things to consider when using them. The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100-kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. To compensate, use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges.

Schottky diode leakage currents and lower dynamic resistances can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DET} slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients than PN junction diodes. After exposure to ESD, Schottky diodes may become shorted or leak. Take care to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

As a general recommendation, use 3-A to 5-A, 100-V rated discrete or bridge diodes for the input rectifiers.

Many high power PoE PD designs require the need for an active FET bridge recitifier in high efficiency applications. An example of an active FET bridge rectifier design can be found in the TPS2373-4EVM-758 User's Guide.

8.2.2.2 Protection, D_1

A TVS, D_1, across the rectified PoE voltage per Figure 30 must be used. TI recommends a SMAJ58A, or equivalent, is recommended for general indoor applications. If an adapter is connected from V_{DD} to RTN, as in ORing option 2 above, then voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

8.2.2.3 Capacitor, C_1

The IEEE 802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 μF to 0.12 μF. Typically a 0.1 μF, 100 V, 10% ceramic capacitor is used.

8.2.2.4 Detection Resistor, R_{DEN}

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} between 23.7 kΩ and 26.3 kΩ, or 25 kΩ ± 5%. A resistor of 24.9 kΩ ± 1% is recommended for R_{DEN}.

8.2.2.5 Classification Resistors, R_{CLSA} and R_{CLSB}

Connect a resistor from CLSA and CLSB to V_{SS} to program the classification current according to the IEEE 802.3bt standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLSA} and R_{CLSB} according to Table 1.

Choose Class 4 for R_{CLSA} = 63.4 Ω.

Choose Class 3 for R_{CLSB} = 90.9 Ω.

8.2.2.6 APD Pin Divider Network R_{APD1}, R_{APD2}

For an adapter voltage threshold to switch from PoE to adapter at 40 V, choose 10 kΩ for R_{APD2}.

$$\frac{V_{Adapter} R_{APD2}}{R_{APD1} + R_{APD2}} = V_{APDEN} \quad (1)$$

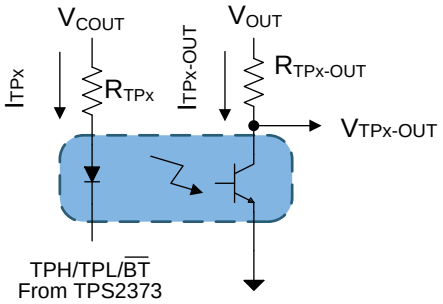
$$\frac{40\ V \times 10\ K\Omega}{10\ K\Omega + R_{APD1}} = 1.65\ V \quad (2)$$

Solving for R_{APD1}:

$$R_{APD1} = 232\ k\Omega \quad (3)$$

8.2.2.7 Opto-isolators for TPH, TPL and $\overline{BT}$

The TPH, TPL and $\overline{BT}$ pin are active-low, open-drain outputs, which give an indication about the PSE allocated power along with its Type. Optocouplers can interface these pins to circuitry on the secondary side of the converter. A high-gain optocoupler and a high-impedance (for example, CMOS) receiver are recommended. Design of the optocoupler interface can be accomplished as follows:



See Table 2 to decode PSE Type

Figure 31. TPH, TPL, and $\overline{BT}$ Interface

1. As shown in Figure 31, let V_{COUT} = 12 V, V_{OUT} = 5 V, $R_{TPx–OUT}$ = 10 kΩ, V_{TPx} = 260 mV, $V_{TPx-OUT}$ = 400 mV.

$$I_{TPx–OUT} = \frac{V_{OUT} - V_{TPx–OUT}}{R_{TPx–OUT}} = \frac{5 - 0.4}{10000} = 0.46\ mA \quad (4)$$

2. The optocoupler current transfer ratio, CTR, is needed to determine R_{TPx}. A device with a minimum CTR of 100% at 1 mA LED bias current, I_{TPx}, is selected. In practice, CTR will vary with temperature, LED bias current, and aging, These variations may require some iteration using the CTR-versus-IDIODE curve on the optocoupler data sheet.
   (a) The approximate forward voltage of the optocoupler diode, V_{FWLED}, is 1.1 V from the data sheet.
   (b) Use Equation 5.

$$I_{TPx\text{-}MIN} = \frac{I_{TPx\text{-}OUT}}{CTR} = \frac{0.46\ mA}{1.00} = 0.46\ mA,\ \text{Select } I_{TPx} = 1\ mA$$
$$R_{TPx} = \frac{V_C - V_{TPx} - V_{FWLED}}{I_{TPx}} = \frac{12\ V - 0.26\ V - 1.1\ V}{1\ mA} = 10.6\ k\Omega \quad (5)$$

(c) Choose a 10.7 kΩ resistor.

8.2.2.8 V_C Input and Output, C_{VCIN} and C_{VCOUT}

The advanced startup circuit requires that C_{VCOUT} ≥ 10 x C_{VCIN}. Using the minimum requirement of C_{VCIN},

C_{VCIN} = 0.1 µF

Choose C_{VCOUT} = 1 µF

The primary switching FETs driven by the PWM controller should be chosen such that its total gate charge is less than 60nC. For gate charges greater than 60nC, C_{OUT} should be increased.

8.2.2.9 UVLO Select, UVLO_SEL

The Design Parameters require the PWM controller UCC2897A which has a UVLO of 8.4 V.

Choose UVLO_SEL to be open circuited

8.2.2.10 Automatic MPS and MPS Duty Cycle, R_{MPS} and R_{MPS_DUTY}

MPS_DUTY should be short circuited to VSS for 12.5% duty cycle

$$R_{MPS} = \frac{V_{AMPS\_CTL}}{I_{MPS}} = \frac{24\,V}{18.5\,mA} = 1.3\,k\Omega \quad (6)$$
$$P_{RMPS} = \frac{V_{MPS}^2}{R_{MPS} \times \text{MPS Duty Cycle}} = \frac{24\,V^2 \times 26.4\%}{1.3k\Omega \times 26.4\%} = 115\,mW \quad (7)$$

Choose 1.3 kΩ rated for 1/8 W

26.4% duty cycle is chosen to take into account if the PD is connected to a IEEE802.3at PSE with a longer MPS timing specification.

8.2.2.11 Internal Voltage Reference, R_{REF}

Per Recommended Operating Conditions,

Choose R_{REF}=49.9 kΩ

8.2.3 Application Curves

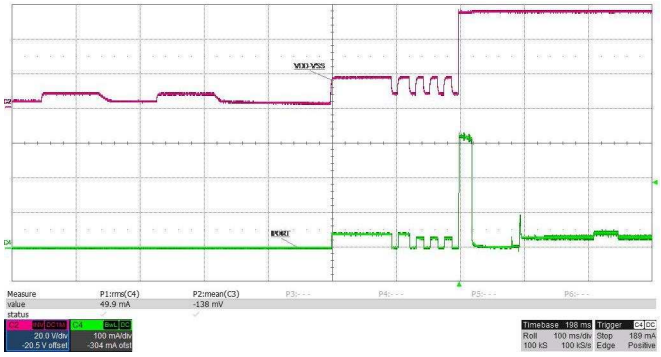


Figure 32. Startup

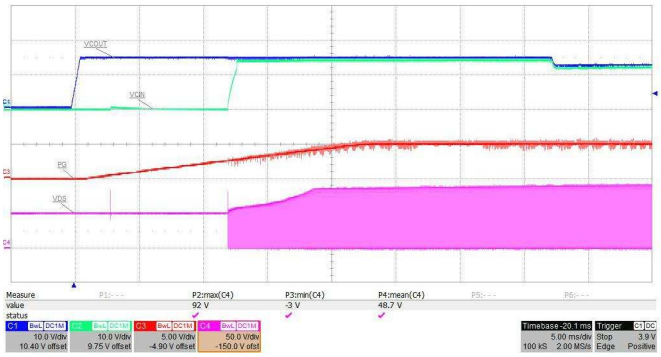


Figure 33. Power Up and Start

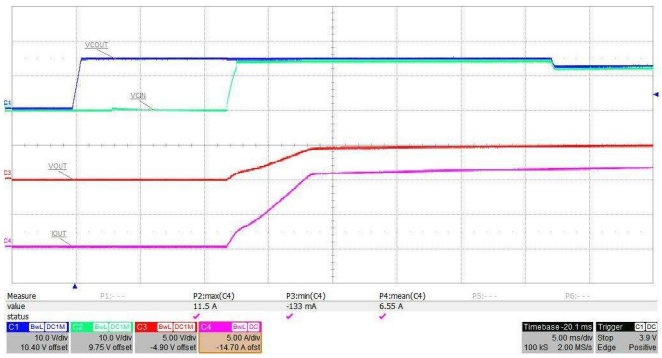


Figure 34. Advanced Startup and Converter Output Startup

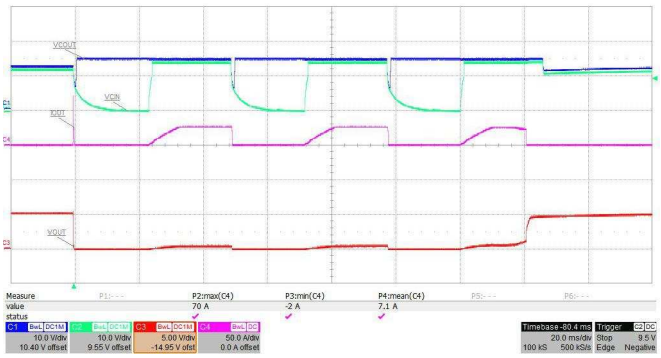


Figure 35. Converter Output Short and Recovery

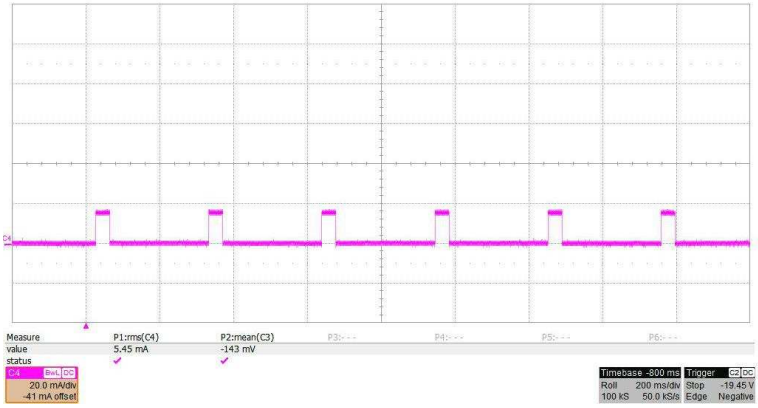


Figure 36. Auto MPS

9 Power Supply Recommendations

The TPS2373 device will typically be followed by a power supply such as an isolated flyback or active clamp forward converter or a non-isolated buck converter. The input voltage of the converter should be capable of operating within the IEEE802.3bt recommended input voltage as shown in Table 6.

10 Layout

10.1 Layout Guidelines

The layout of the PoE front end should follow power and EMI/ESD best practice guidelines. A basic set of recommendations include:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1-µF capacitor, and TPS2373.
- All leads should be as short as possible with wide power traces and paired signal and return.
- There should not be any crossovers of signals from one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS2373 should be located over split, local ground planes referenced to VSS for the PoE input and to RTN for the switched output.
- Large copper fills and traces should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.
- Nine vias are recommended on the Exposed Thermal Pad of the TPS2373. These should connect to all layers of a copper plane on the PCB. Ensure 80% printed solder coverage by area.

10.2 Layout Example

Figure 37 and Figure 38 show the top and bottom layer and assemblies of the TPS2373-4EVM-758 as a reference for optimum parts placement. A detailed PCB layout can be found in the user's guide of the *TPS2373-4EVM-758 Evaluation Module* (SLUUBJ1).

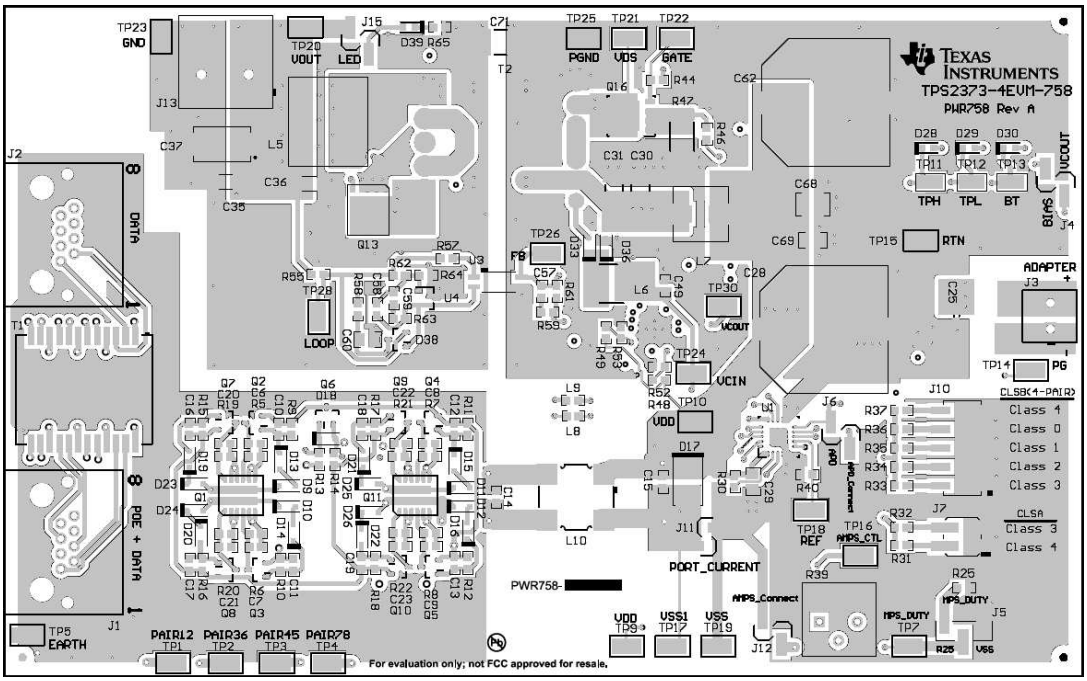


Figure 37. TPS2373-4EVM-758 Top Side Layout and Component Placement

Layout Example (continued)

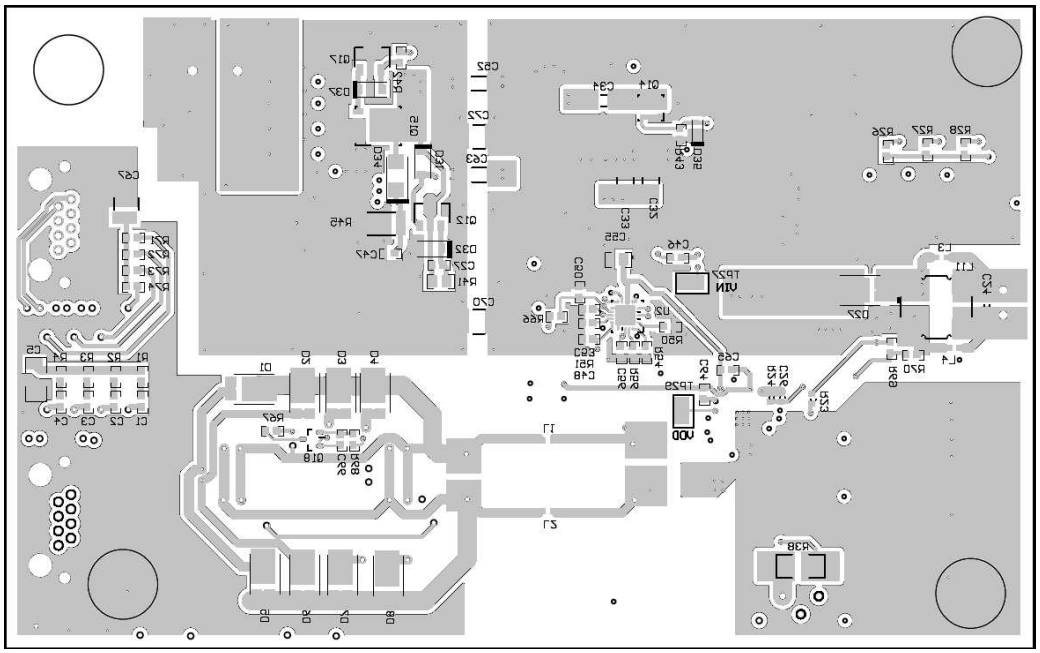


Figure 38. TPS2373-4EVM-758 Bottom Side Layout and Component Placement

10.3 EMI Containment

- Use compact loops for dv/dt and di/dt circuit paths (power loops and gate drives).
- Use minimal, yet thermally adequate, copper areas for heat sinking of components tied to switching nodes (minimize exposed radiating surface).
- Use copper ground planes (possible stitching) and top layer copper floods (surround circuitry with ground floods).
- Use 4 layer PCB if economically feasible (for better grounding).
- Minimize the amount of copper area associated with input traces (to minimize radiated pickup).
- Use Bob Smith terminations, Bob Smith EFT capacitor, and Bob Smith plane.
- Use Bob Smith plane as ground shield on input side of PCB (creating a phantom or literal earth ground).
- Use of ferrite beads on input (allow for possible use of beads or 0 ohm resistors).
- Maintain physical separation between input-related circuitry and power circuitry (use ferrite beads as boundary line).
- Possible use of common-mode inductors.
- Possible use of integrated RJ-45 jacks (shielded with internal transformer and Bob Smith terminations).
- End-product enclosure considerations (shielding).

10.4 Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS2373 is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS2373 device to experience an OTSD event if it is excessively heated by a nearby device.

10.5 ESD

ESD requirements for a unit that incorporates the TPS2373 have a much broader scope and operational implications than are used in TI's testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS2373.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Advanced Adapter ORing Solutions using the TPS23753*, SLVA306

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
TPS2373-4RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS 2373
TPS2373-4RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	TPS 2373

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

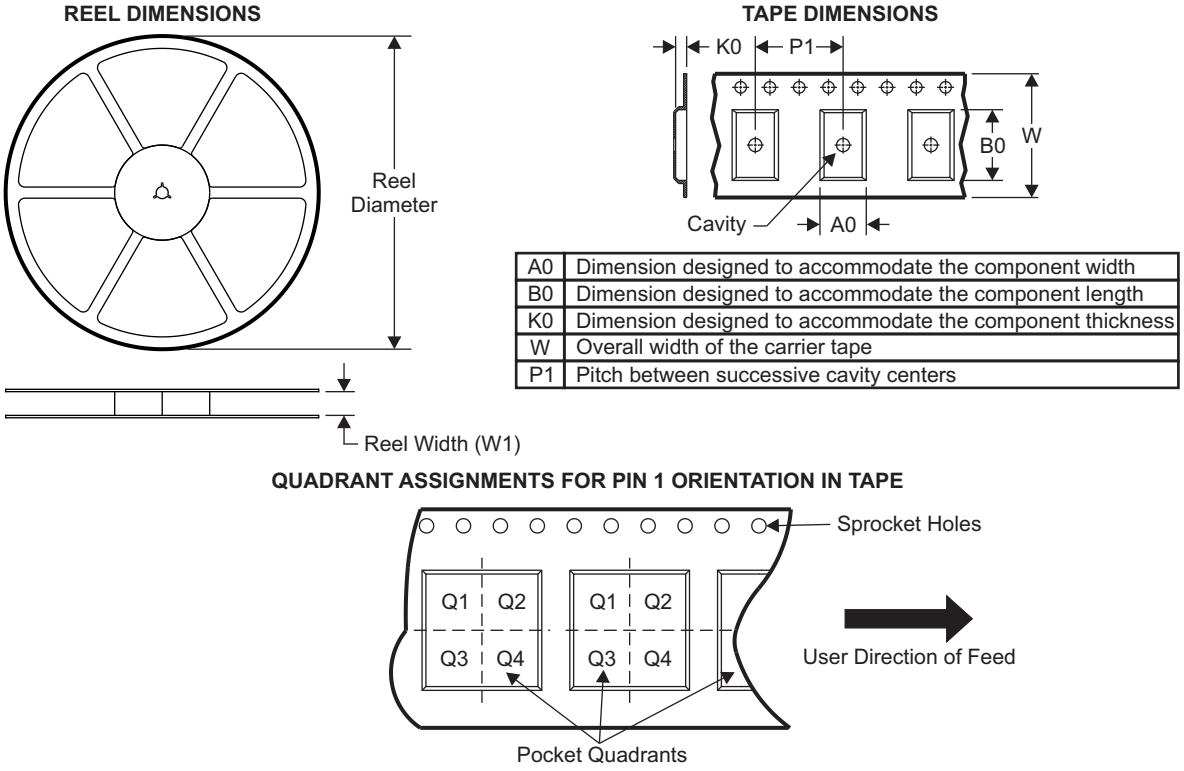
(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

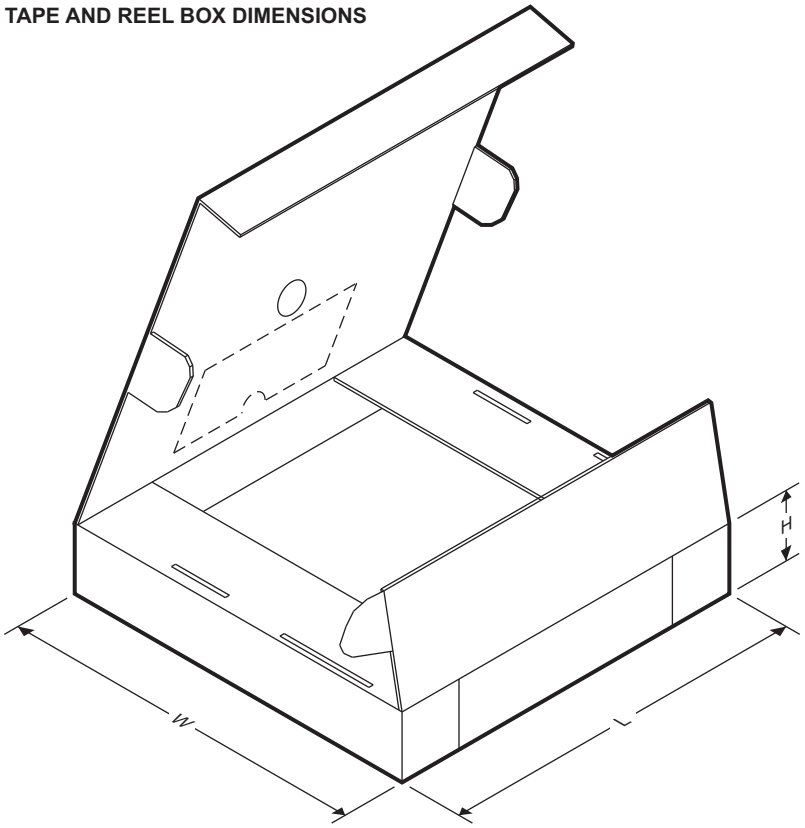
12.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2373-4RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS2373-4RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

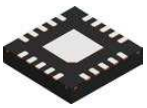
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2373-4RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS2373-4RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

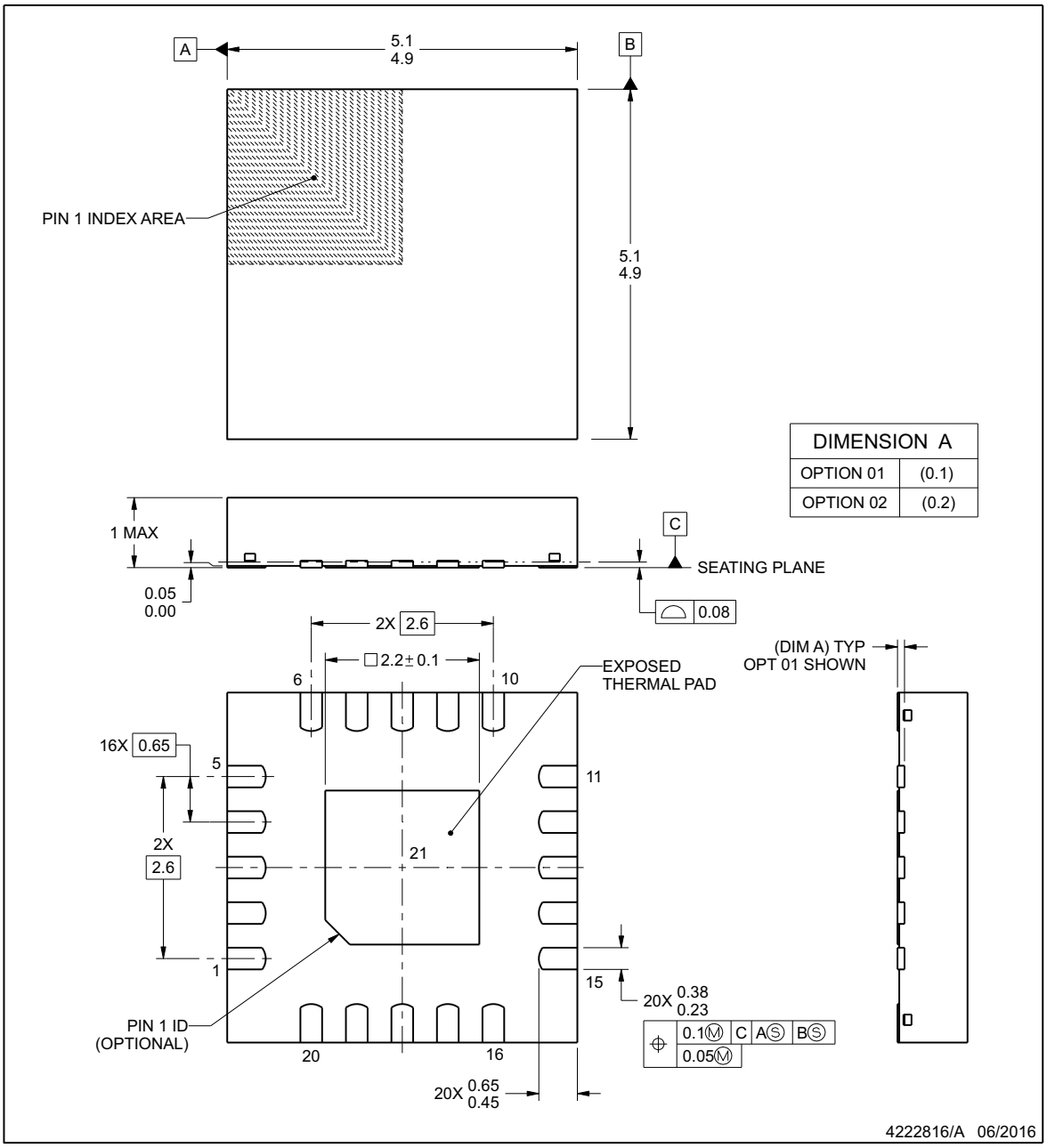
PACKAGE OUTLINE

RGW0020B



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



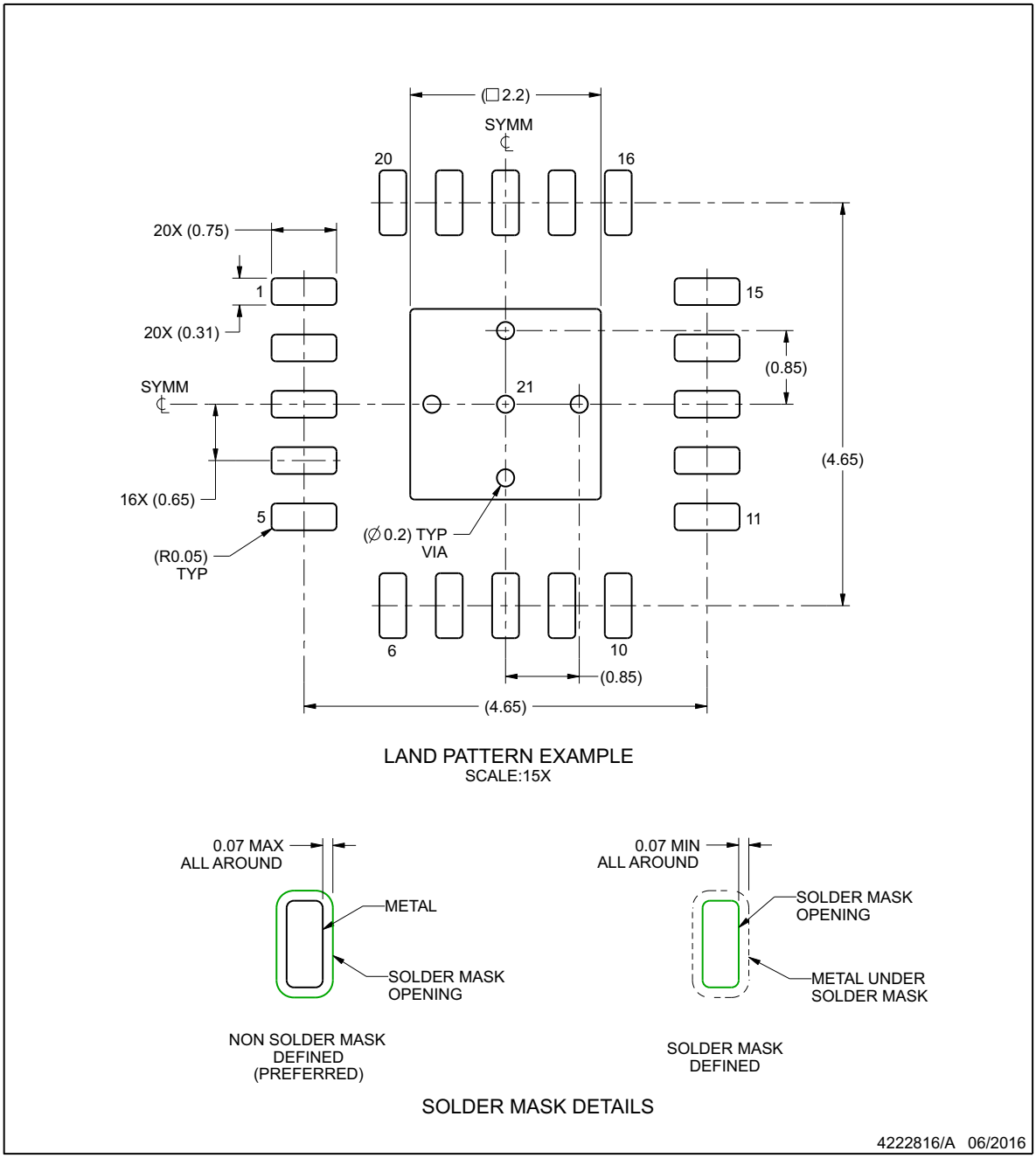
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGW0020B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

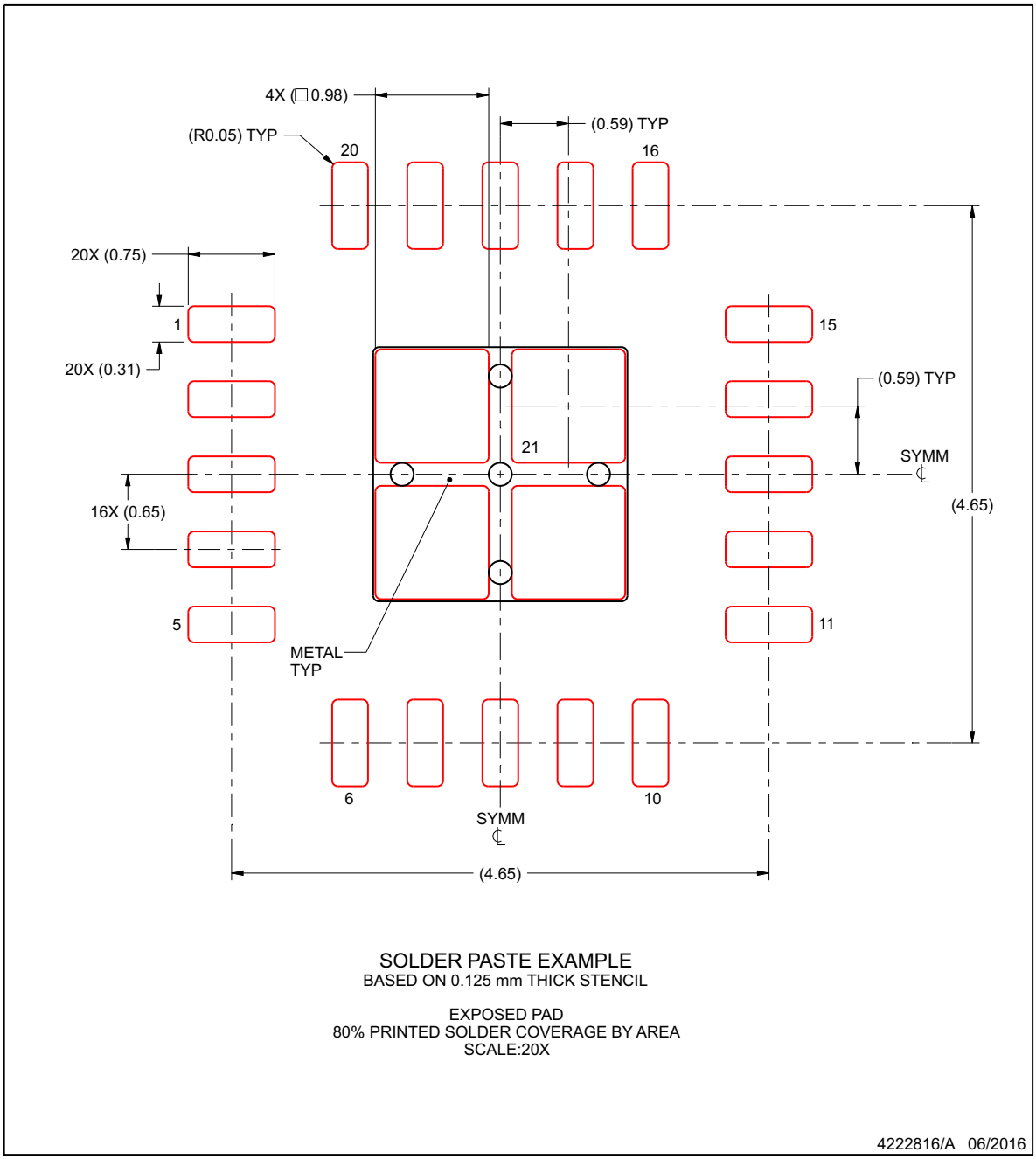
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGW0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222816/A 06/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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